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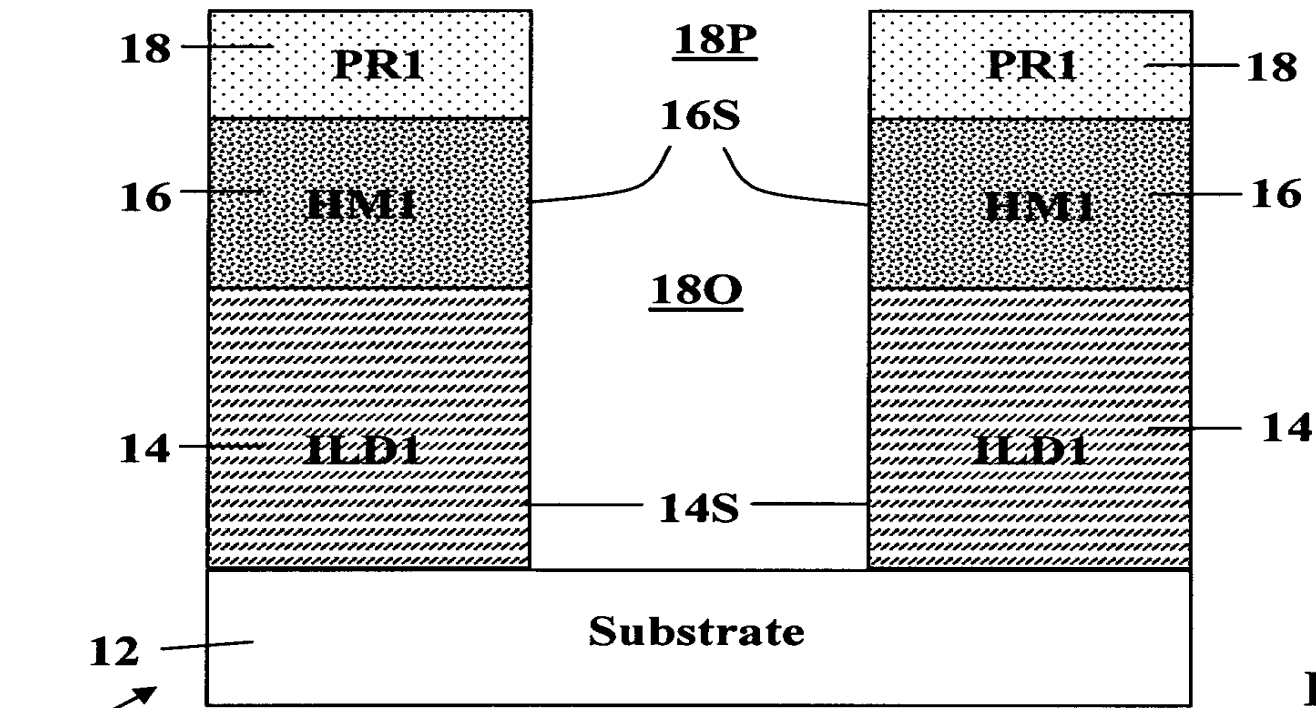


FIG. 1C

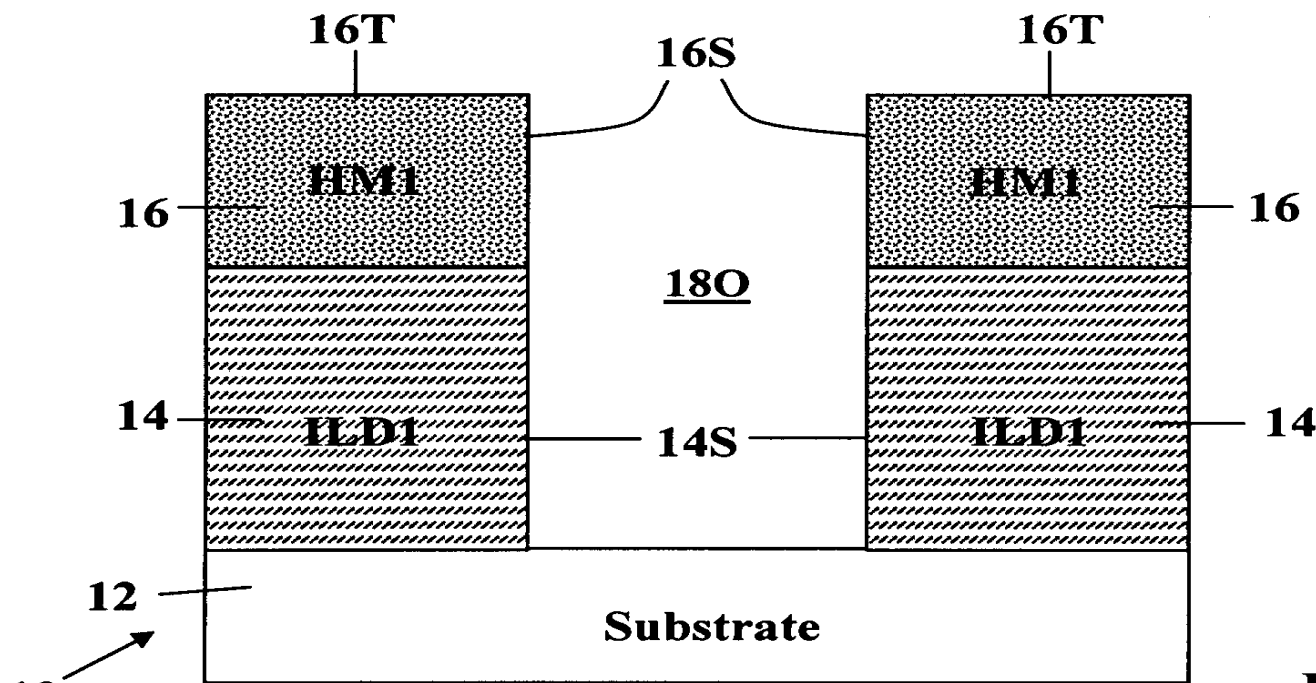
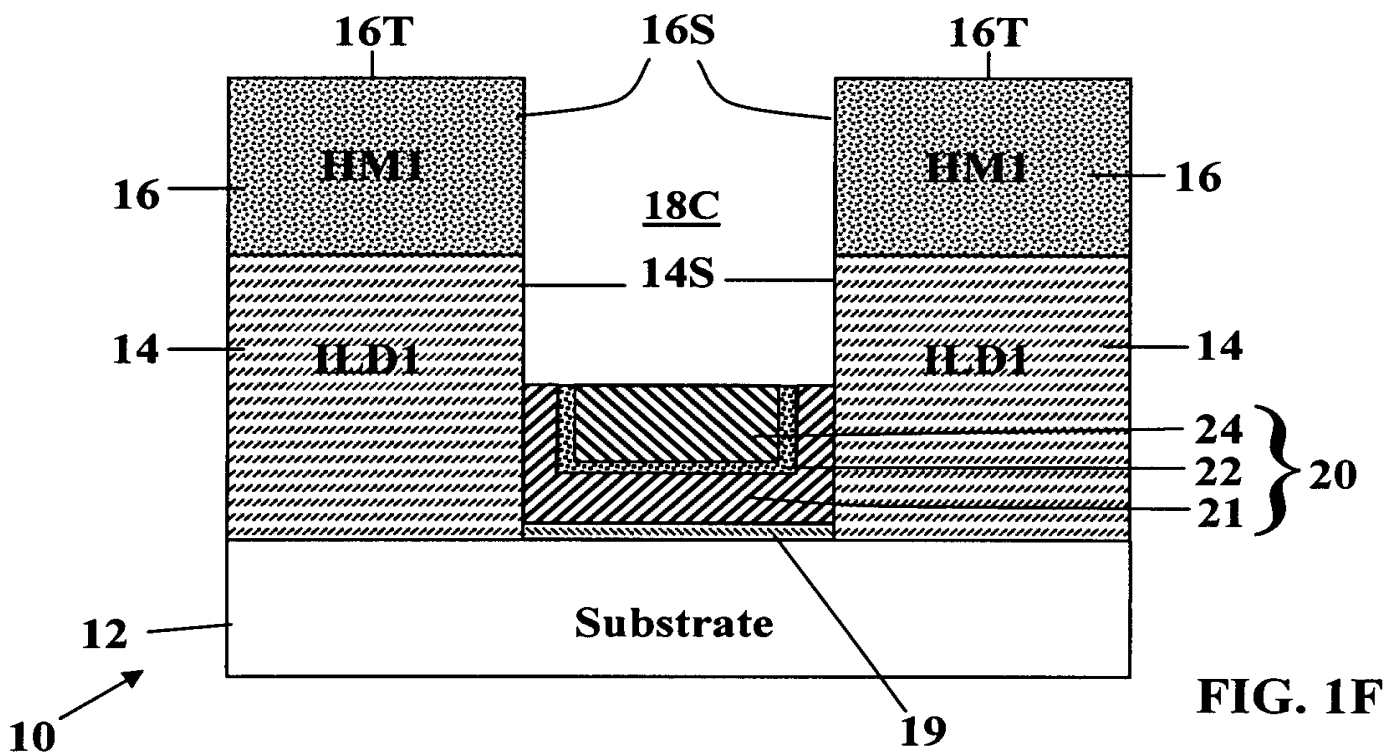
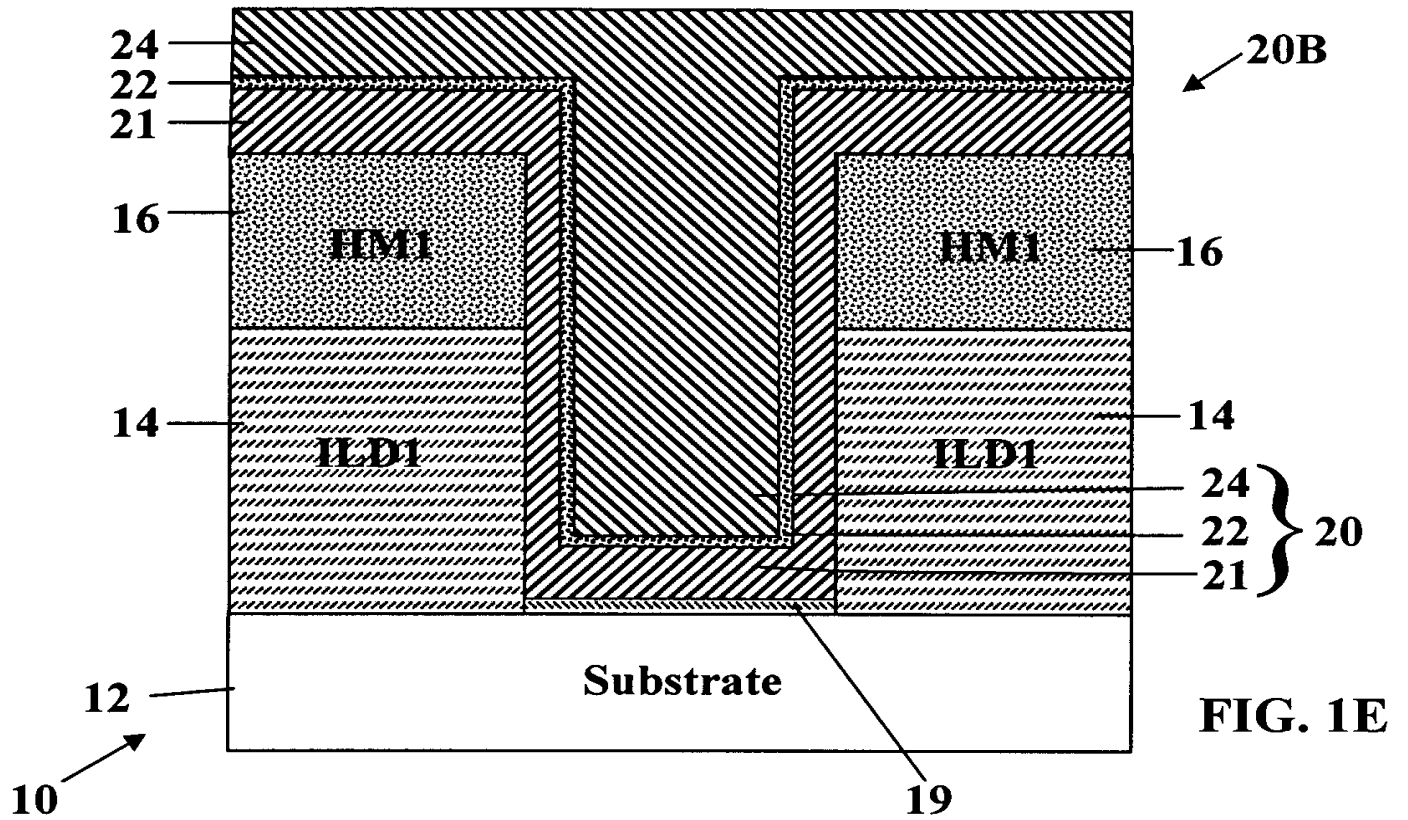
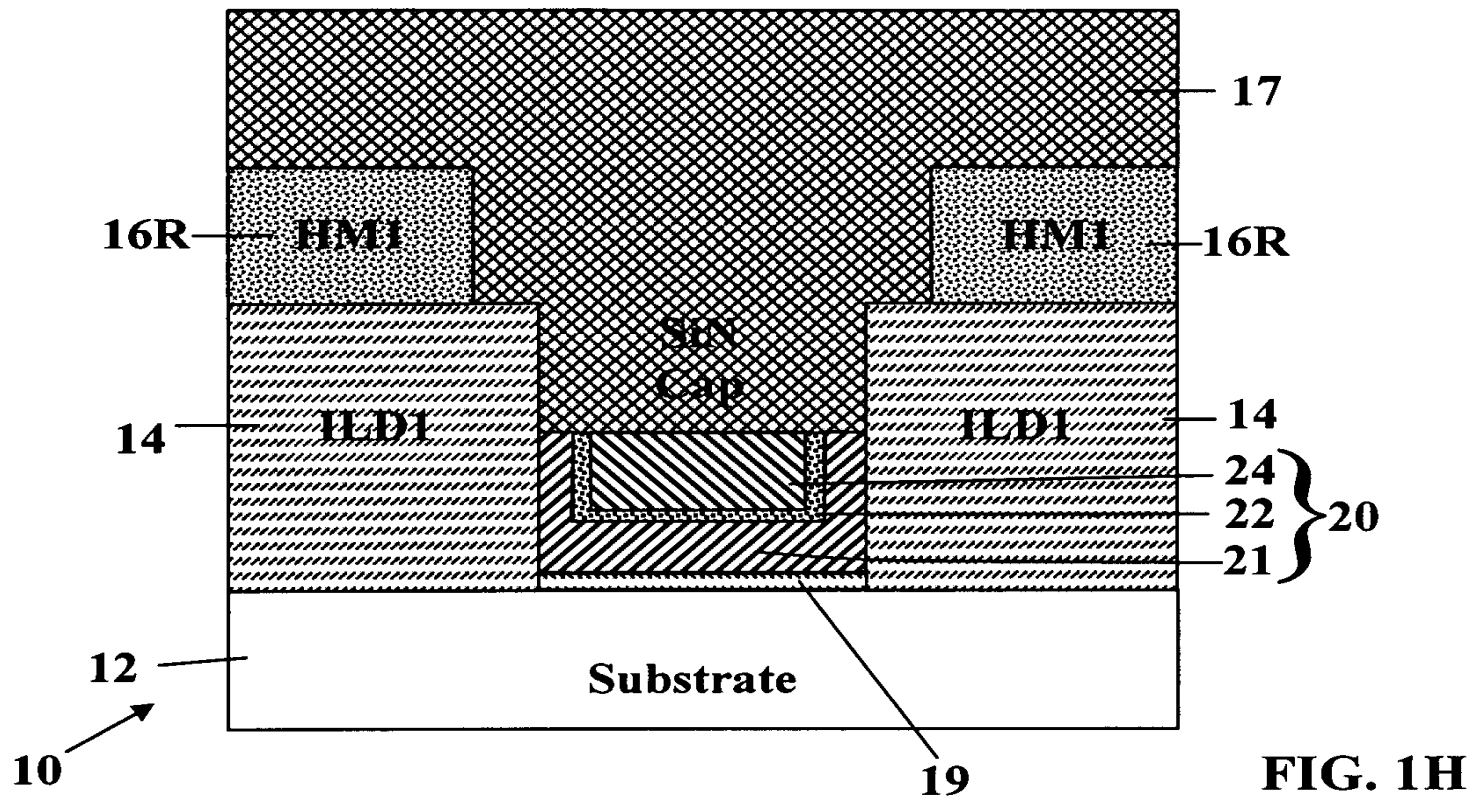
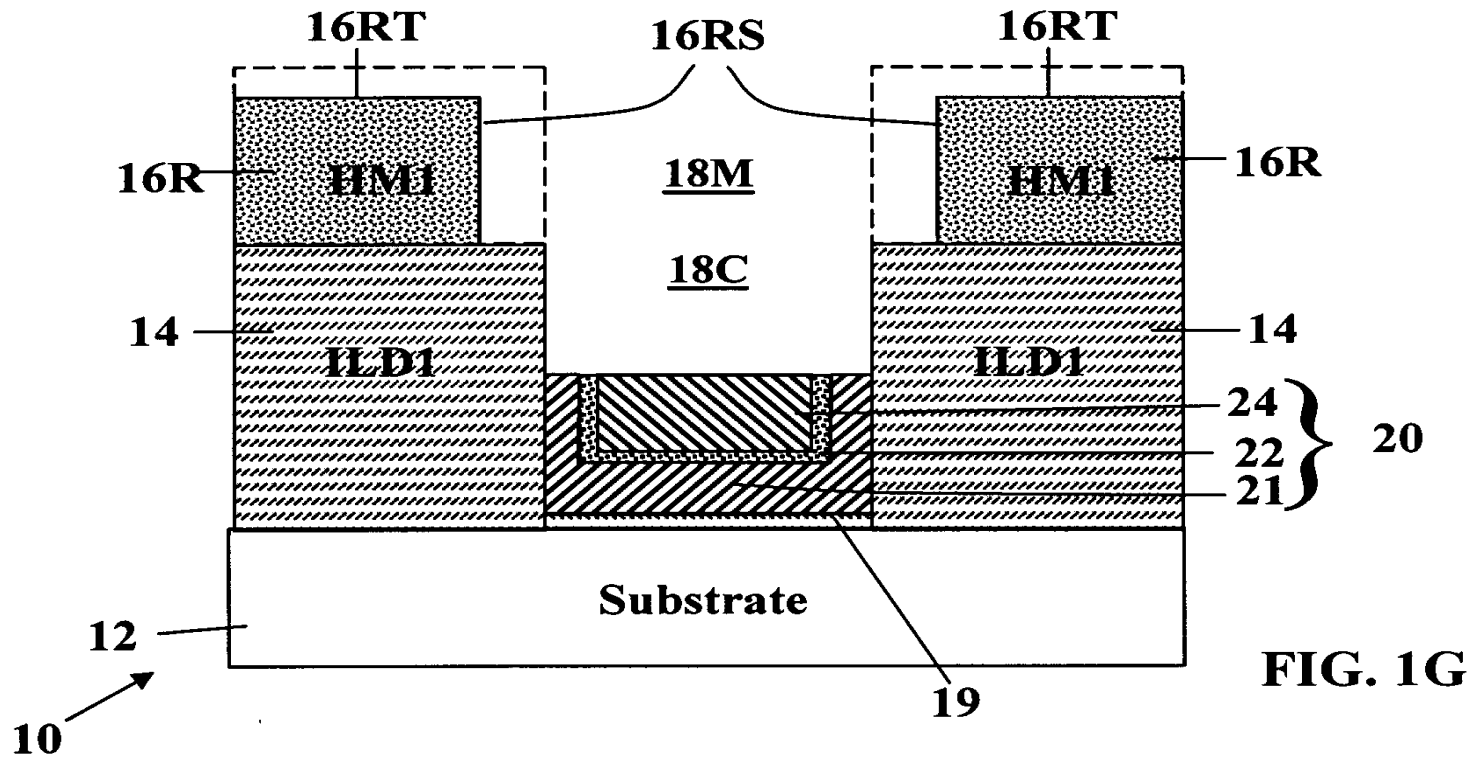
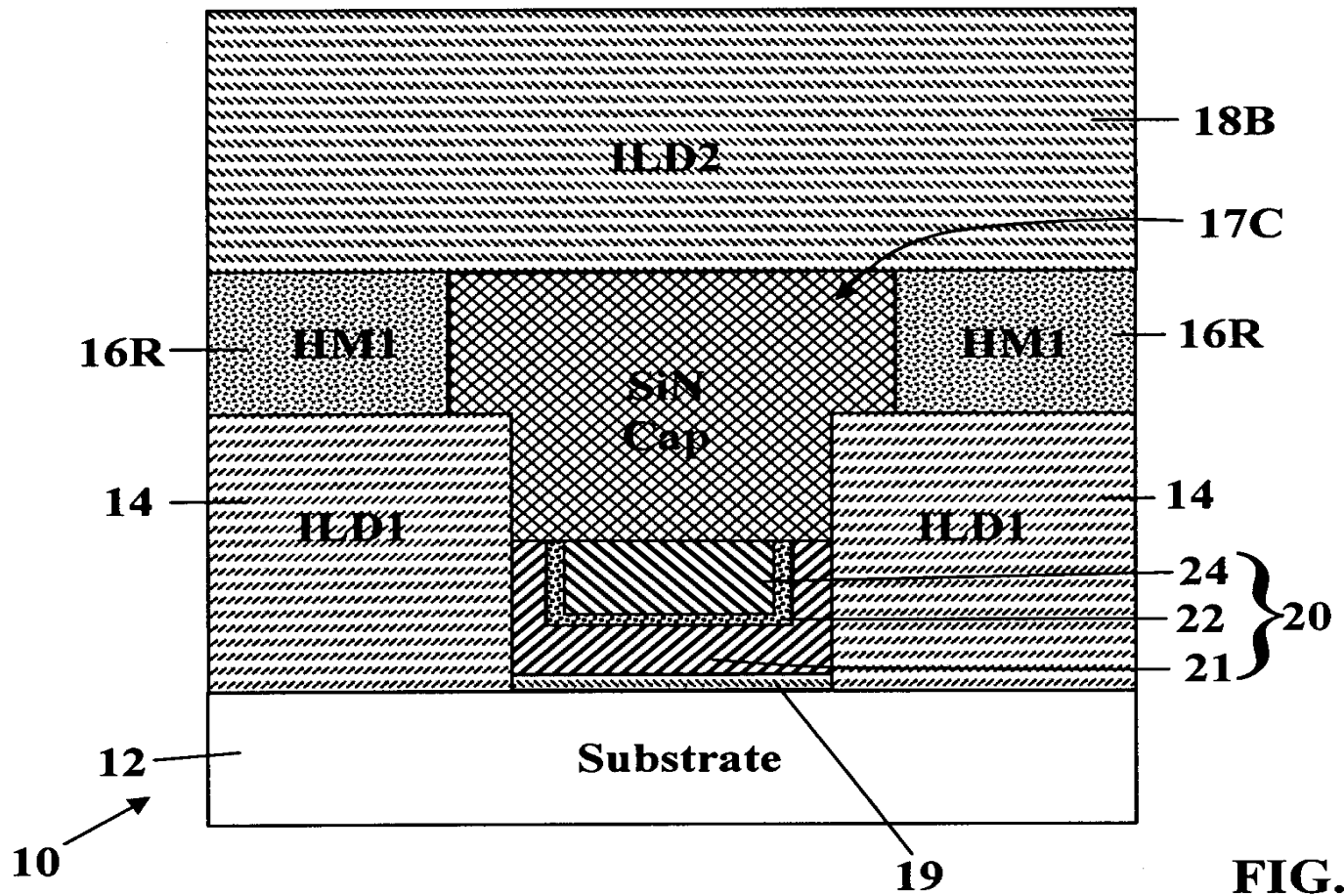
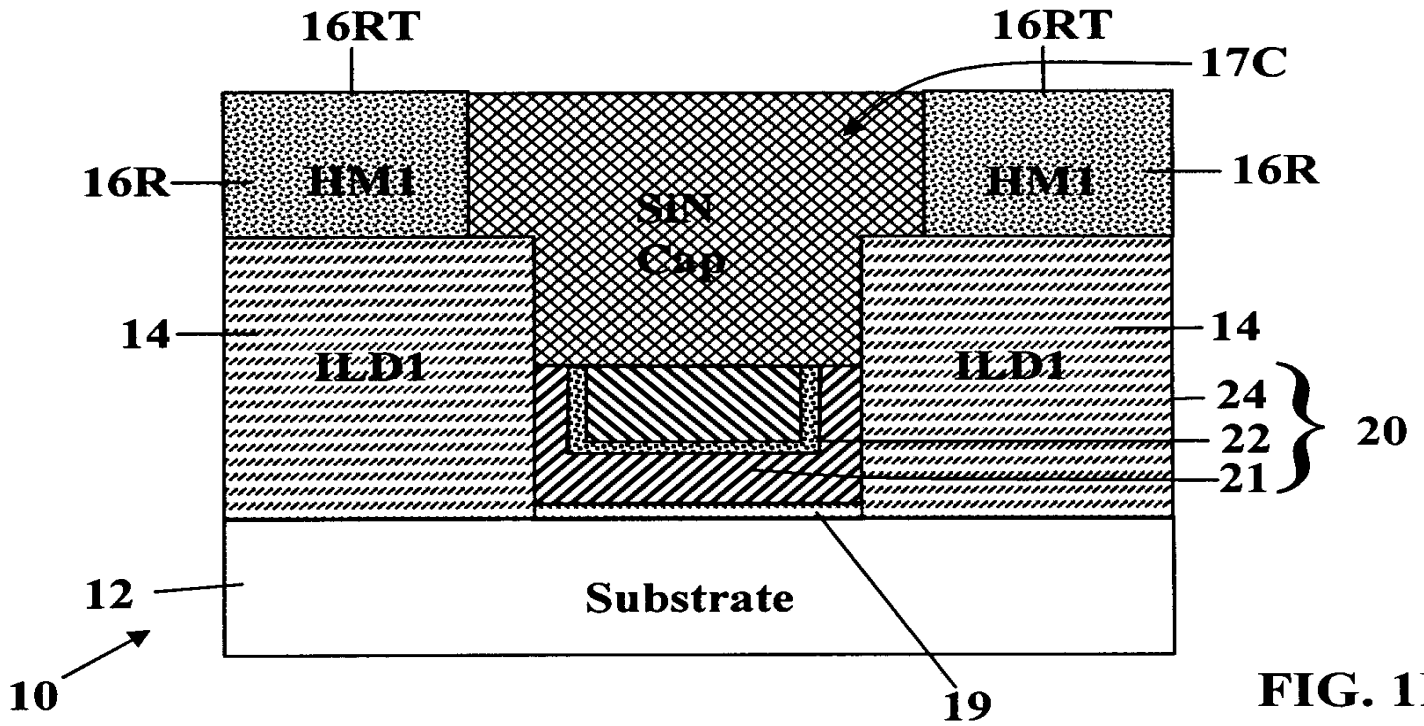


FIG. 1D



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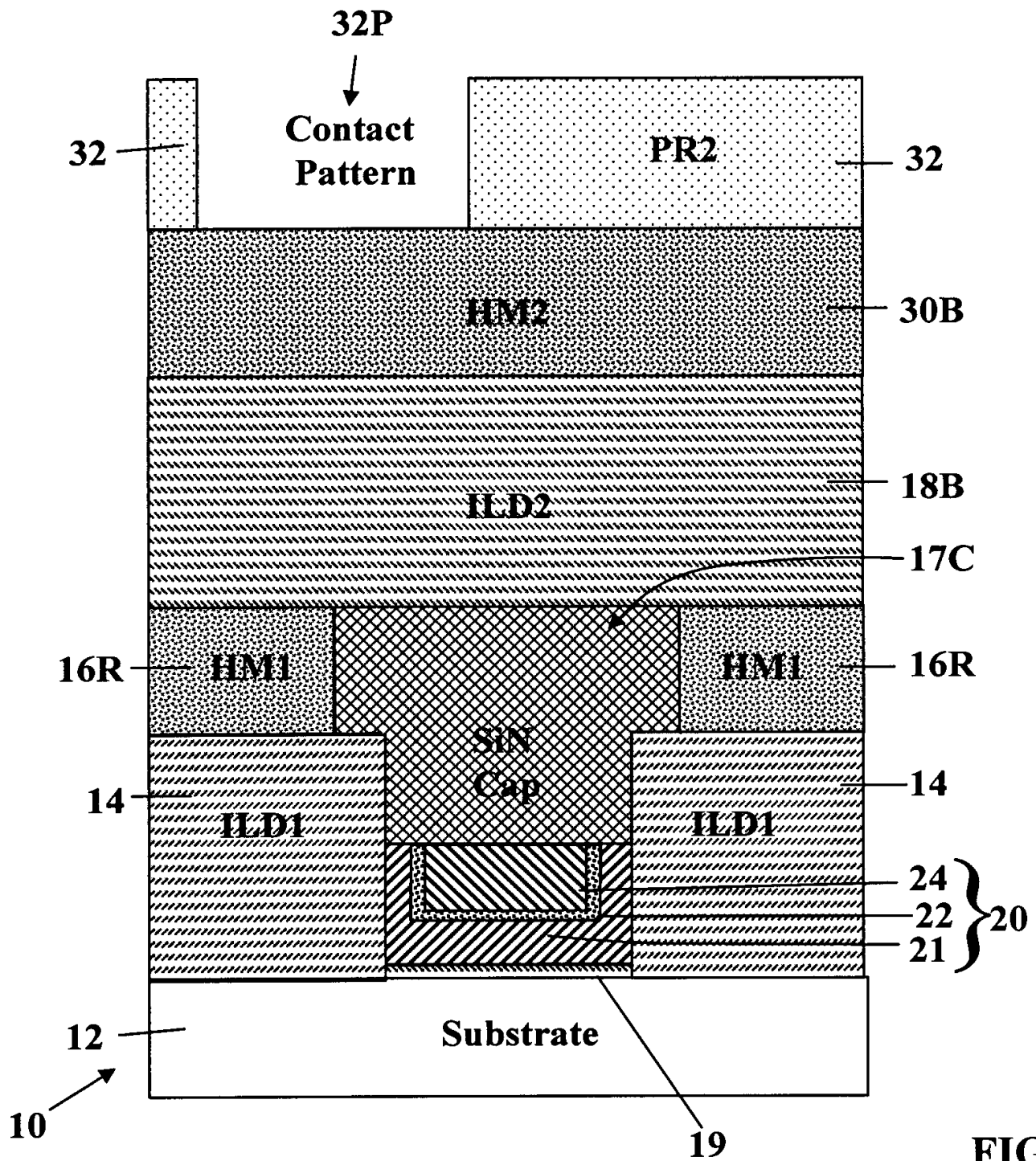


FIG. 1K

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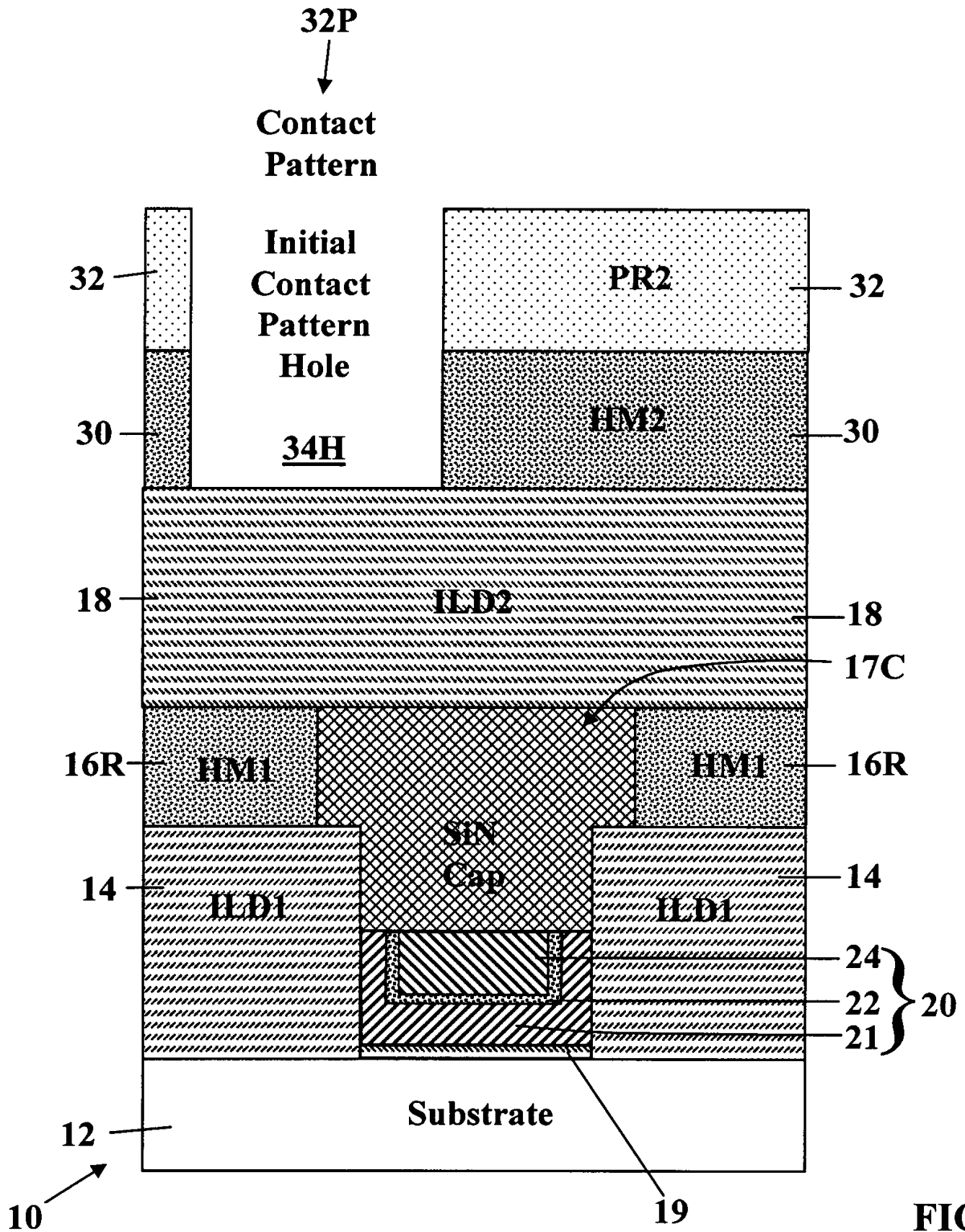


FIG. 1L



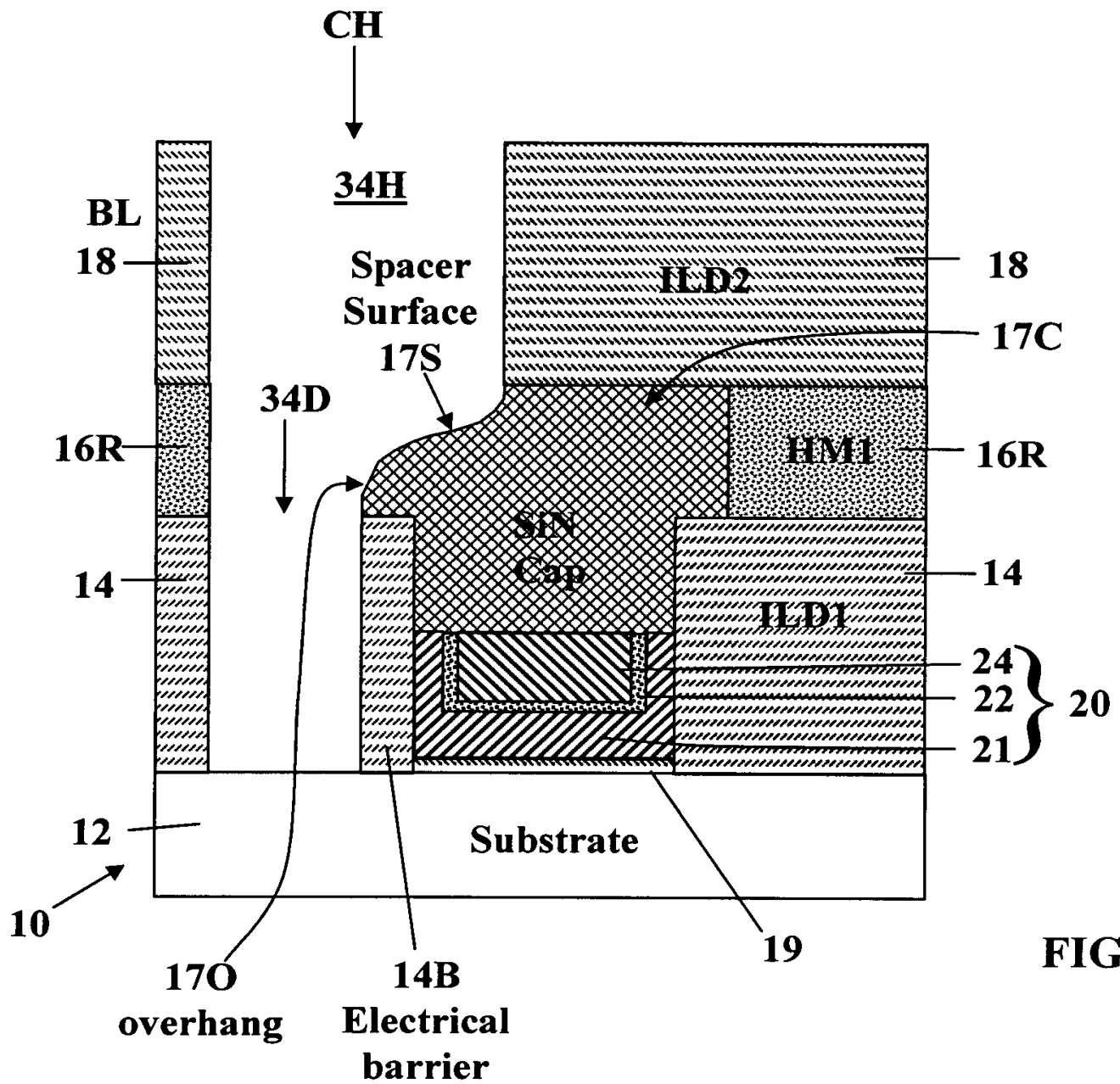


FIG. 1N

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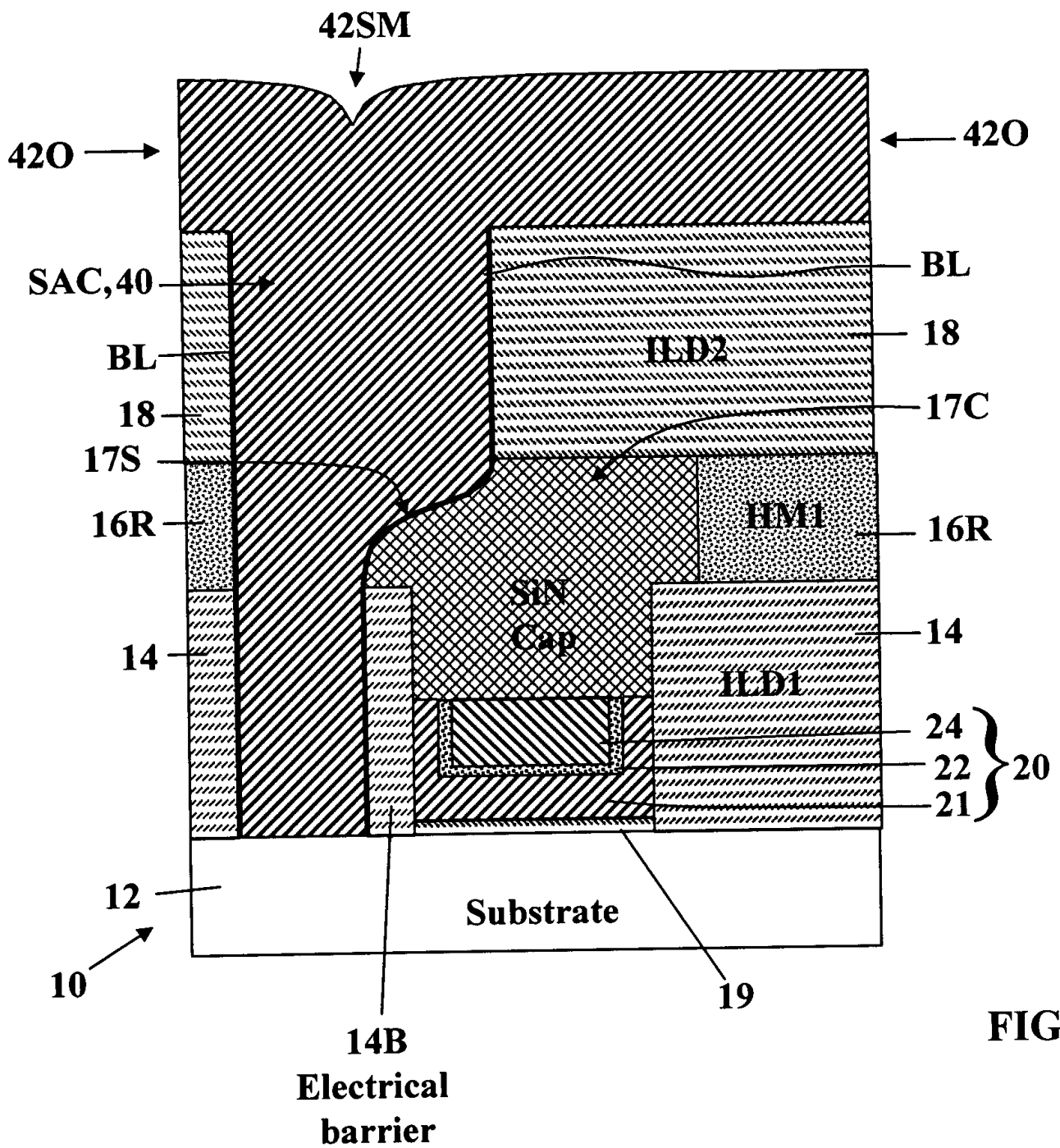
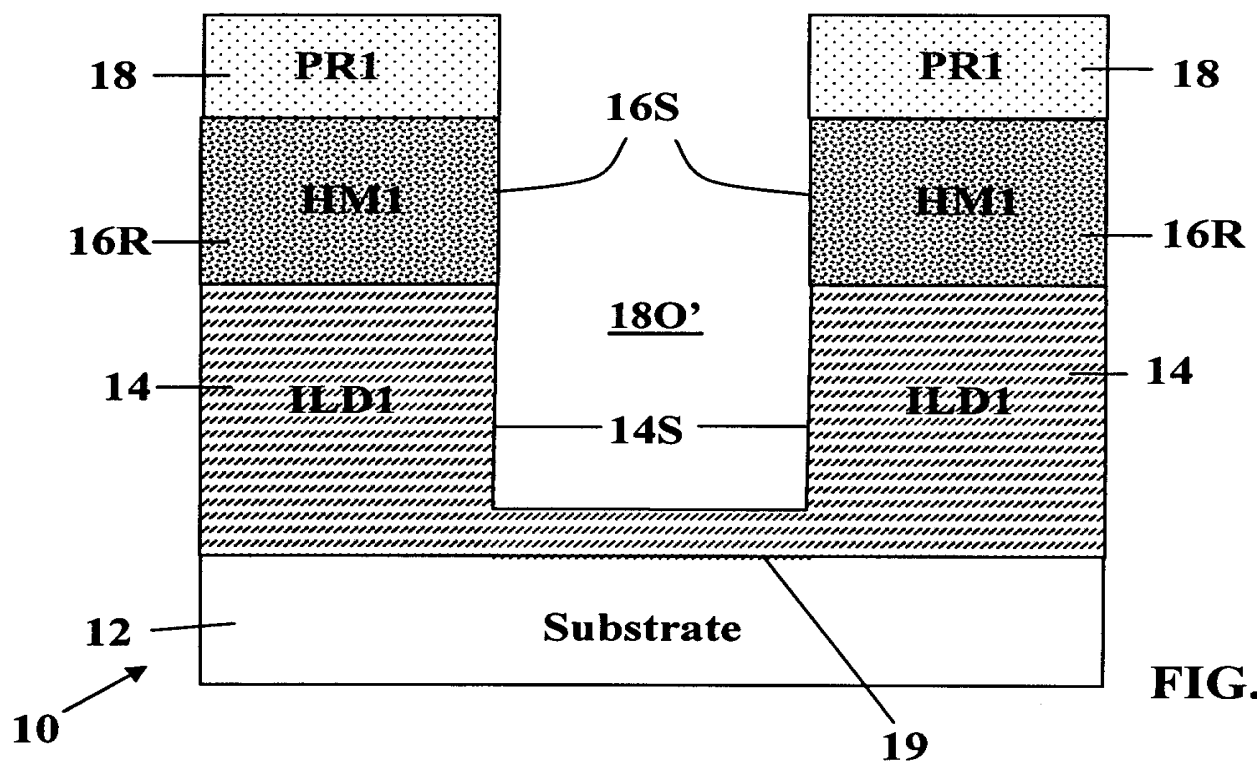
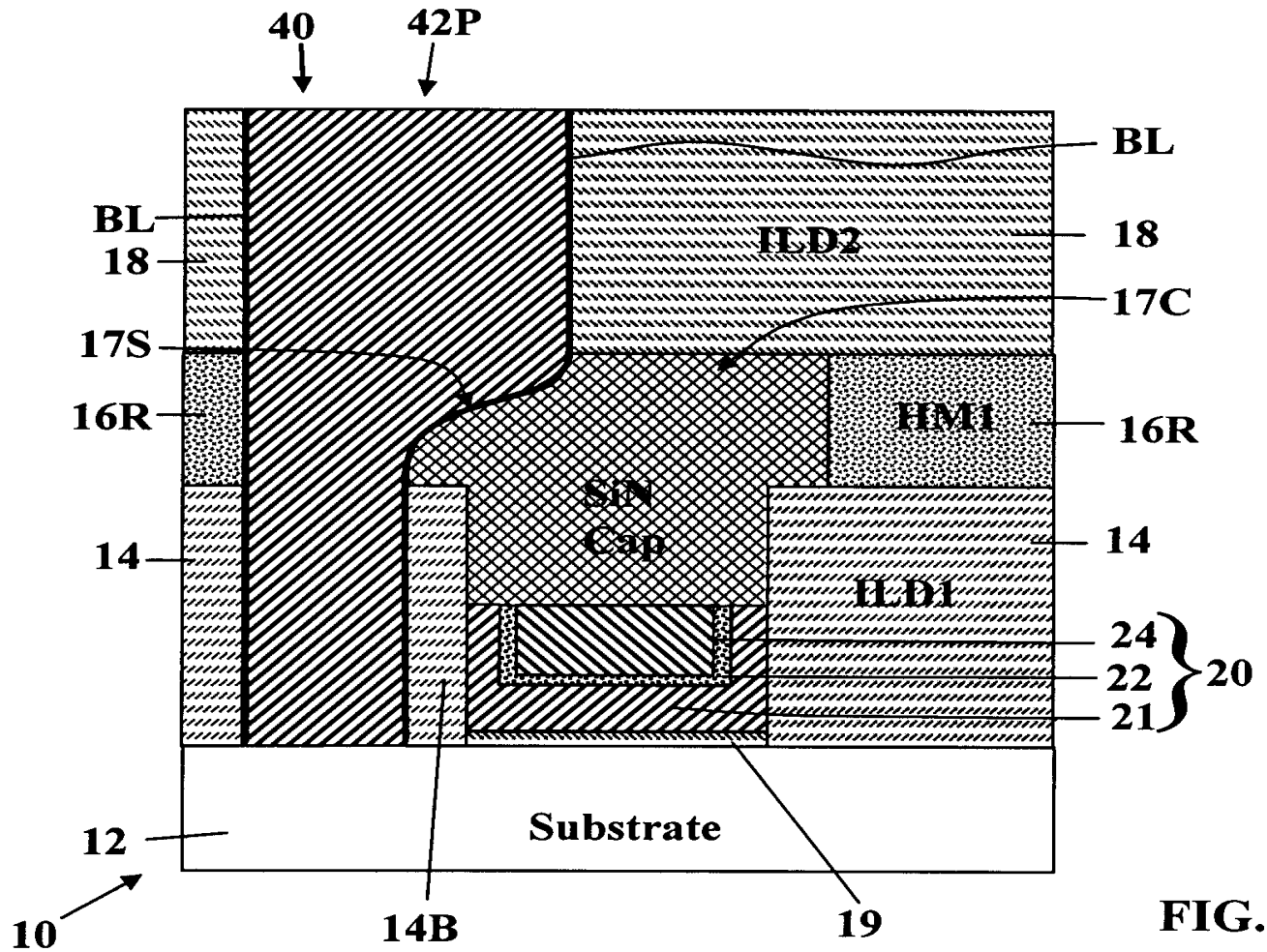
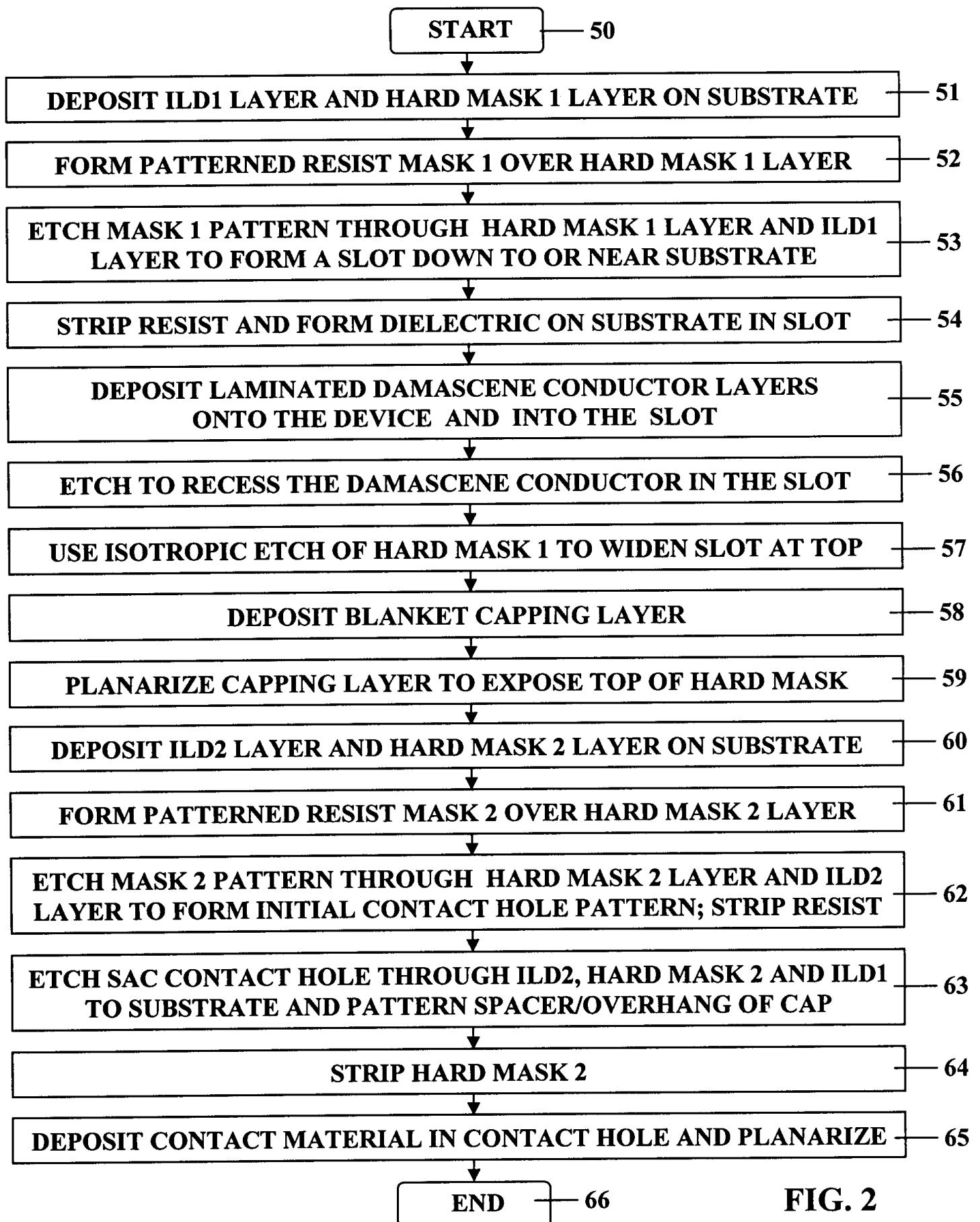
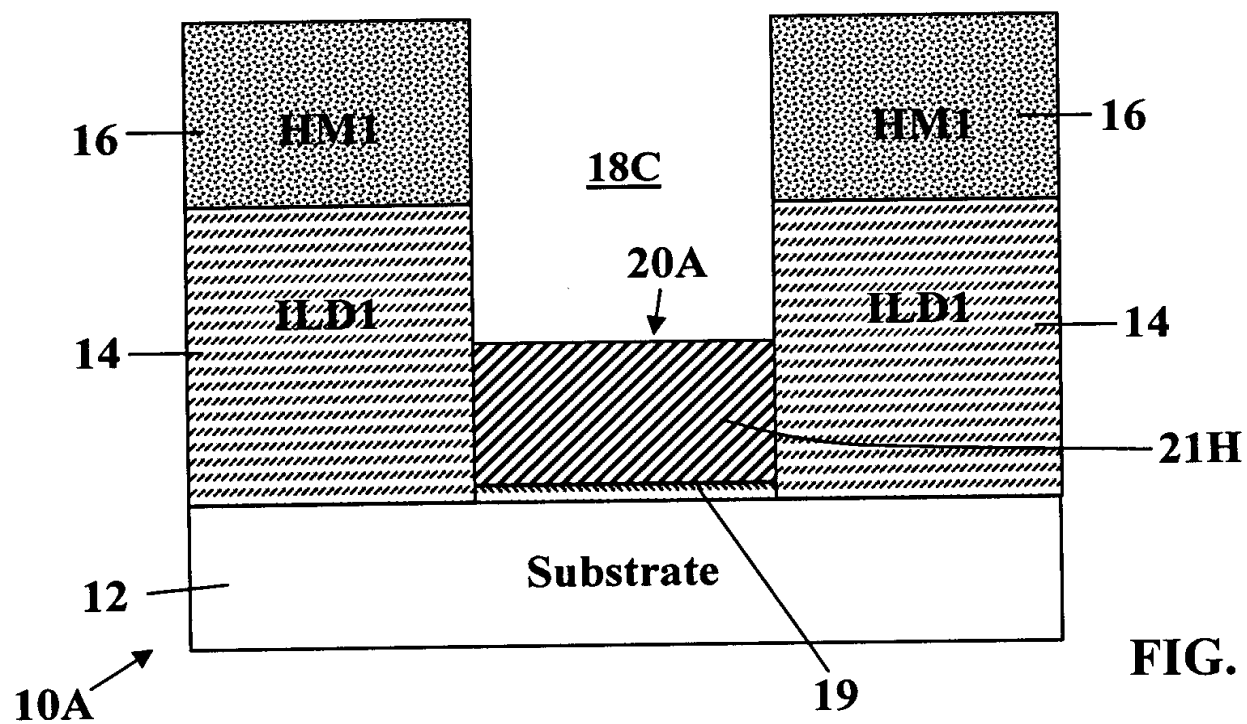
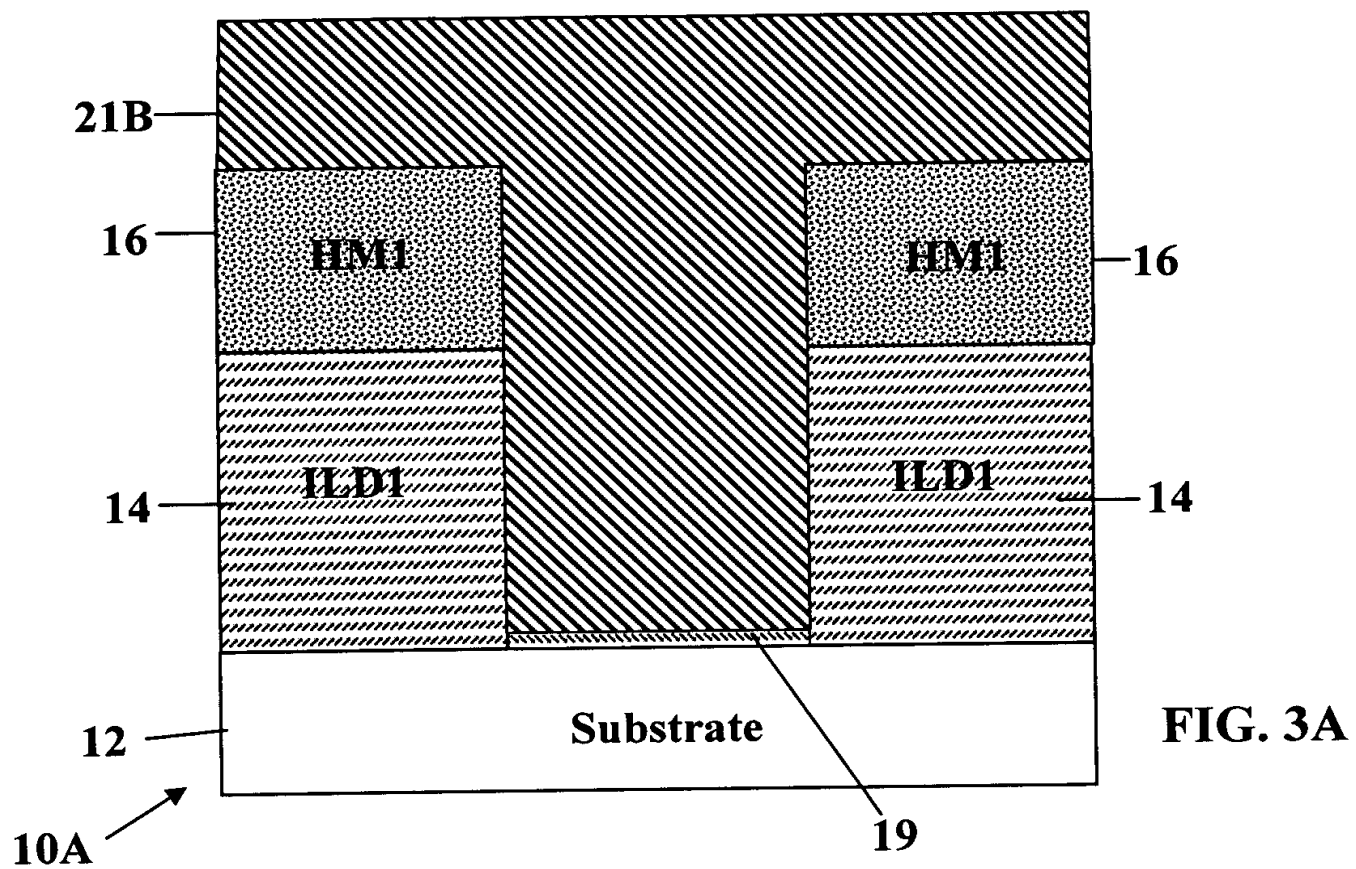


FIG. 10



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**FIG. 2**



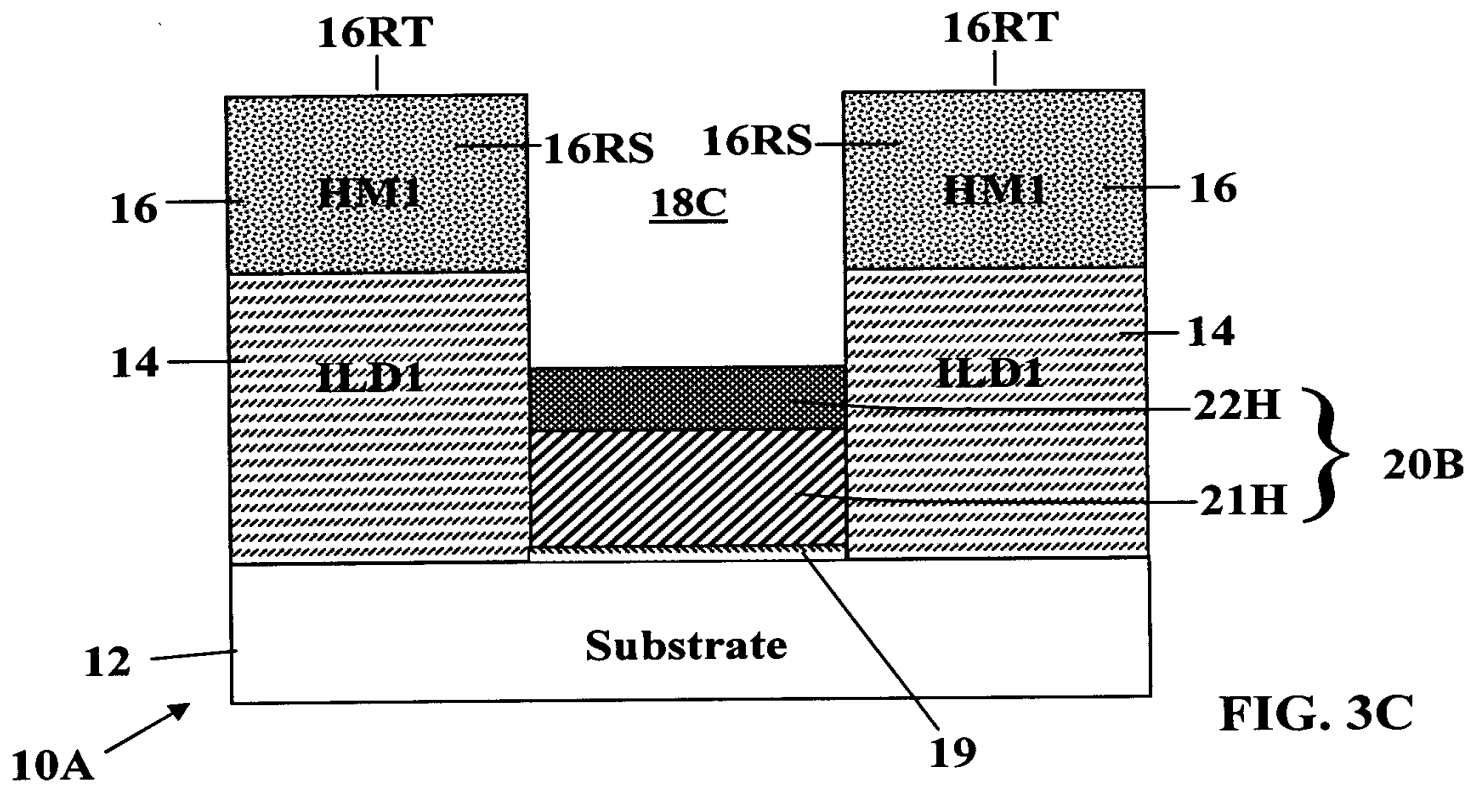


FIG. 3C

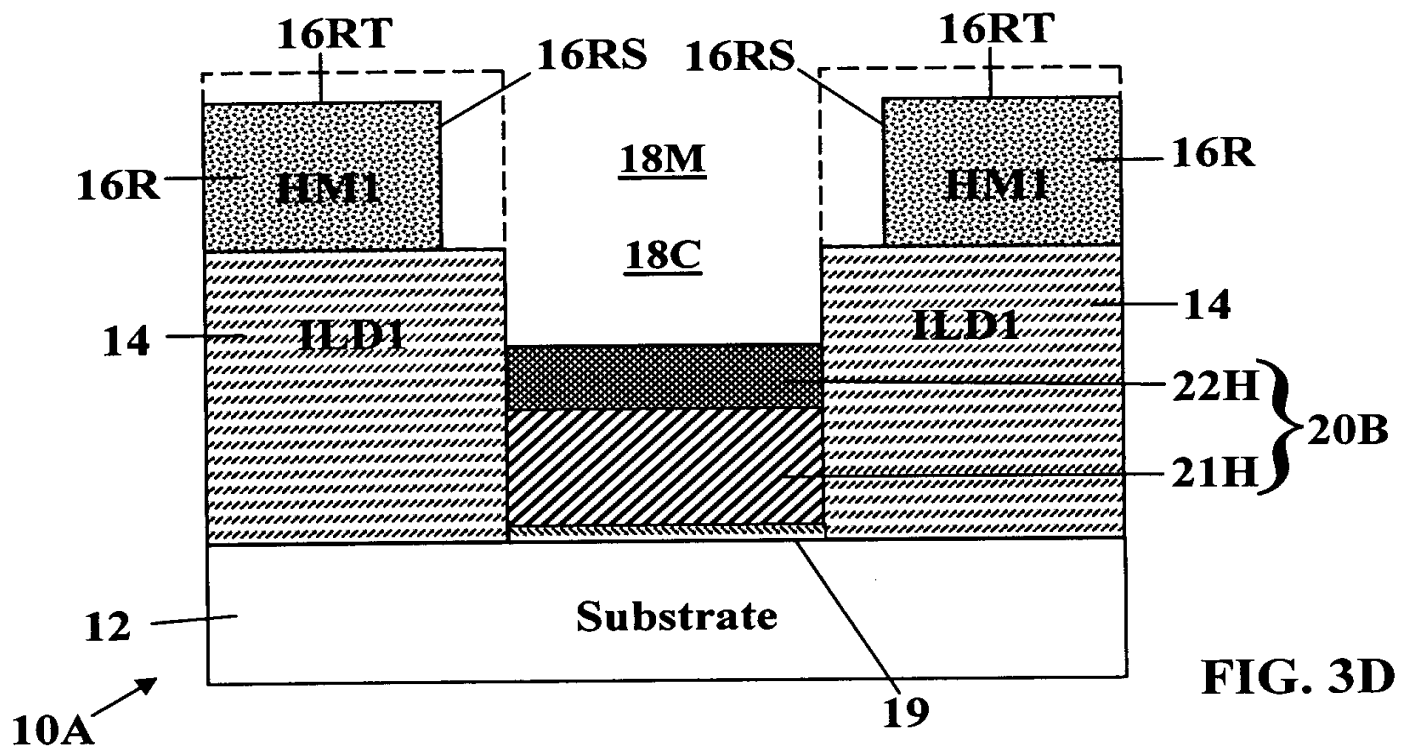
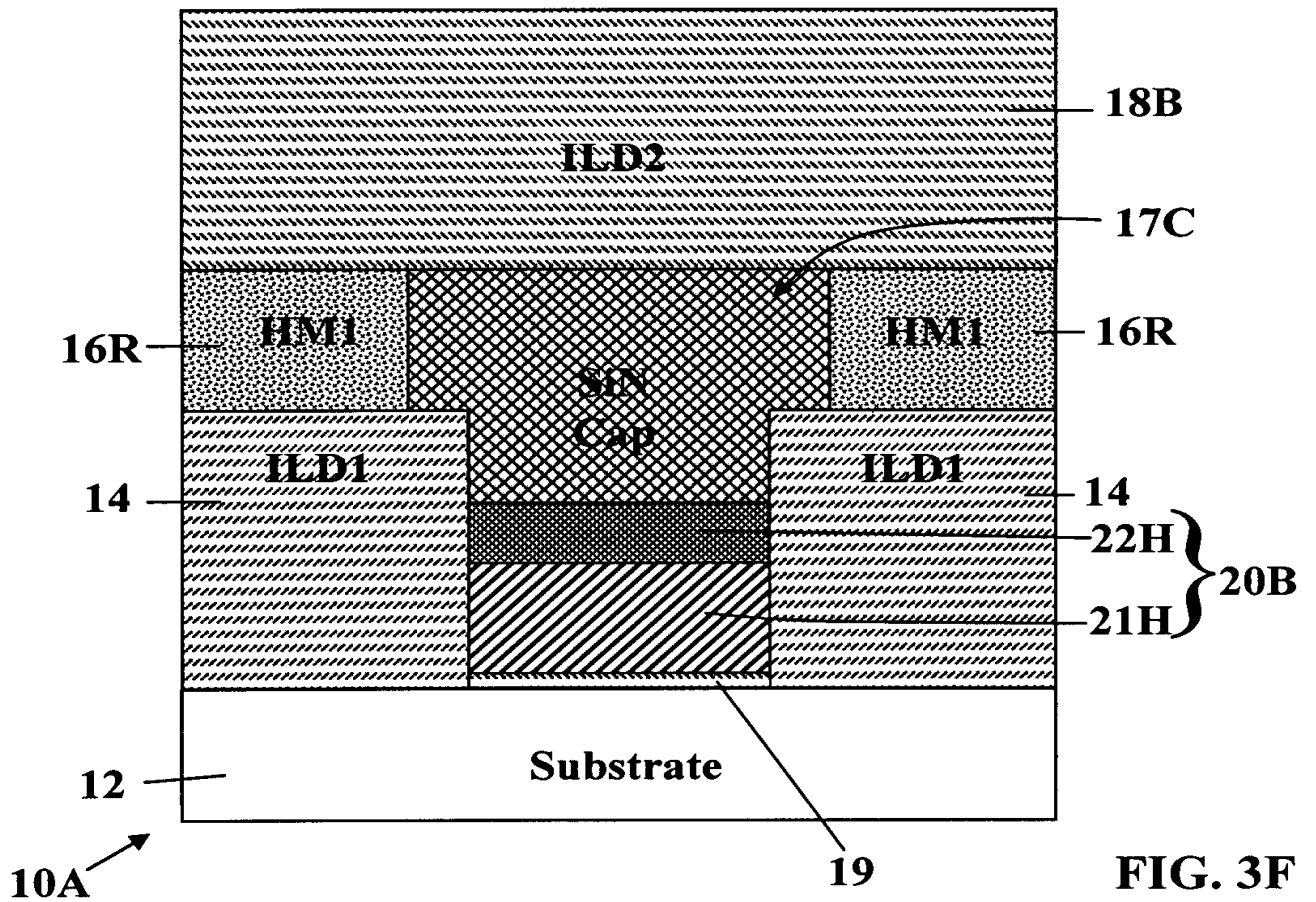
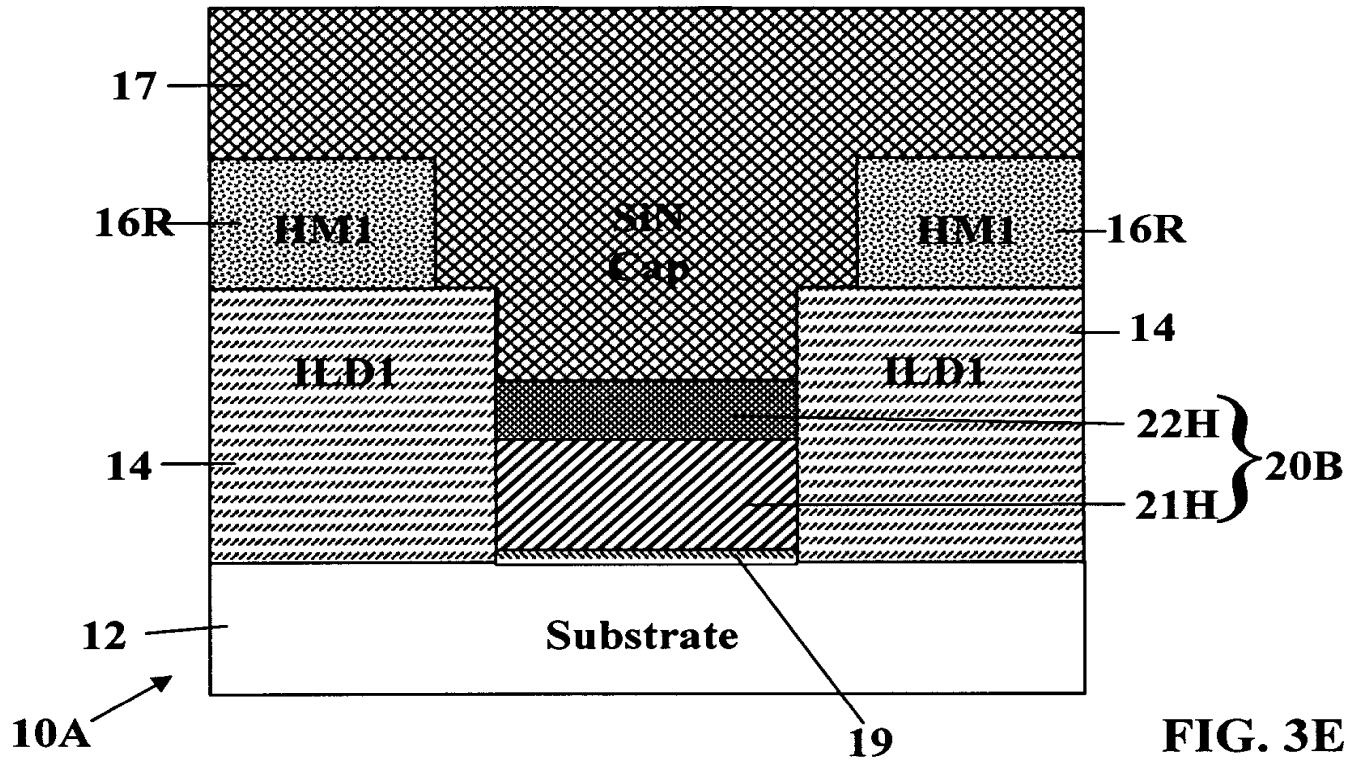


FIG. 3D

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4.1



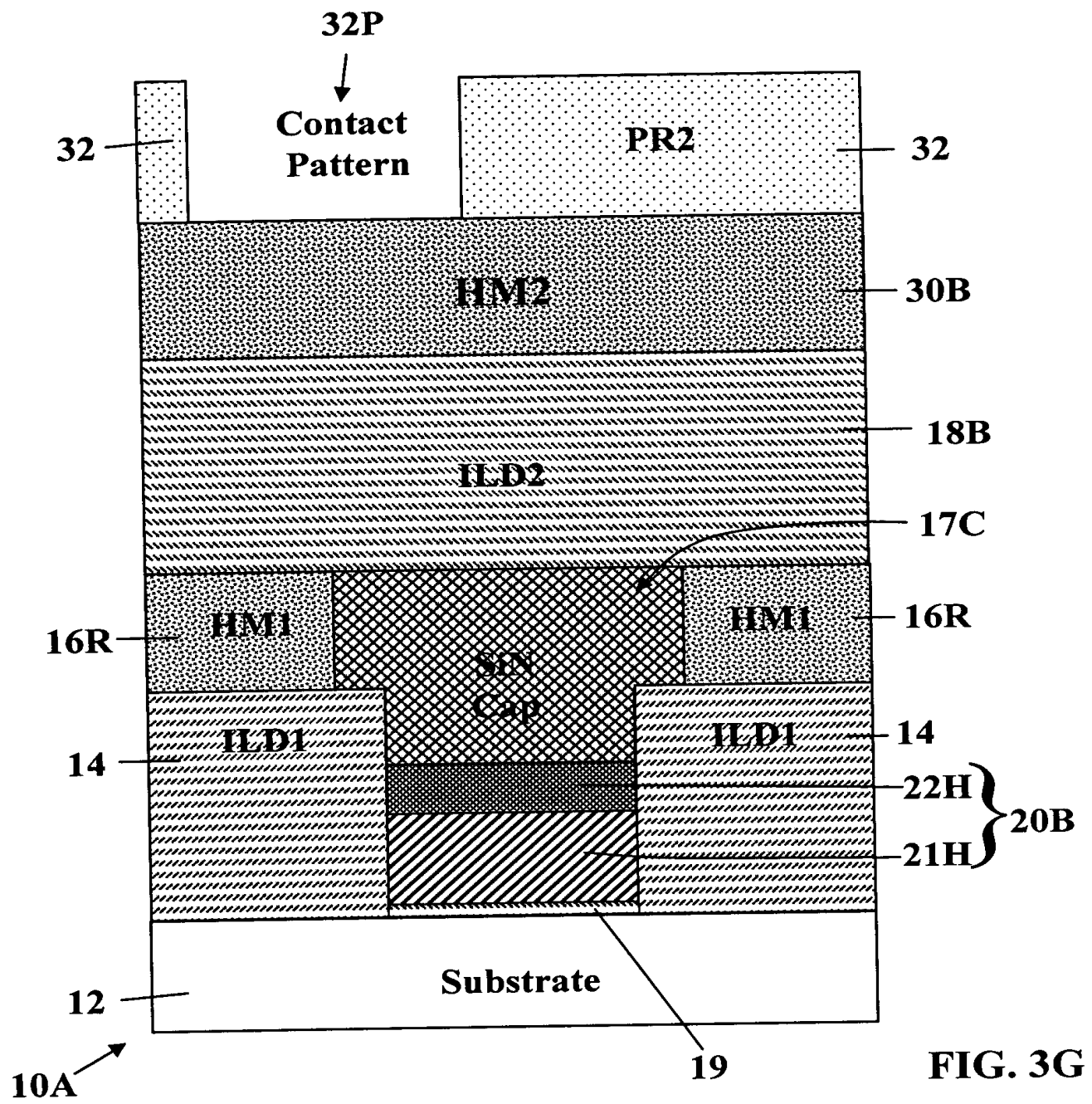


FIG. 3G

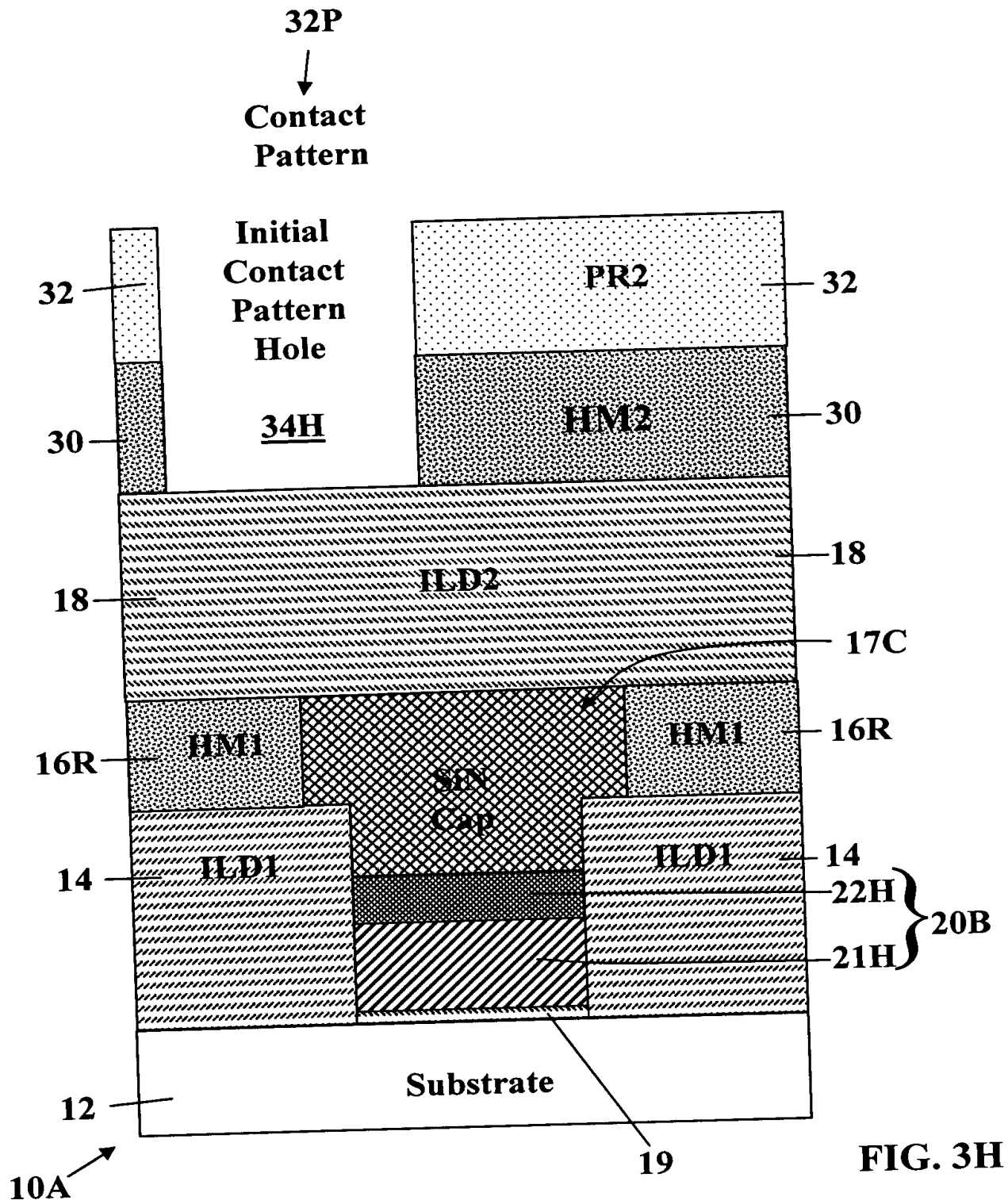
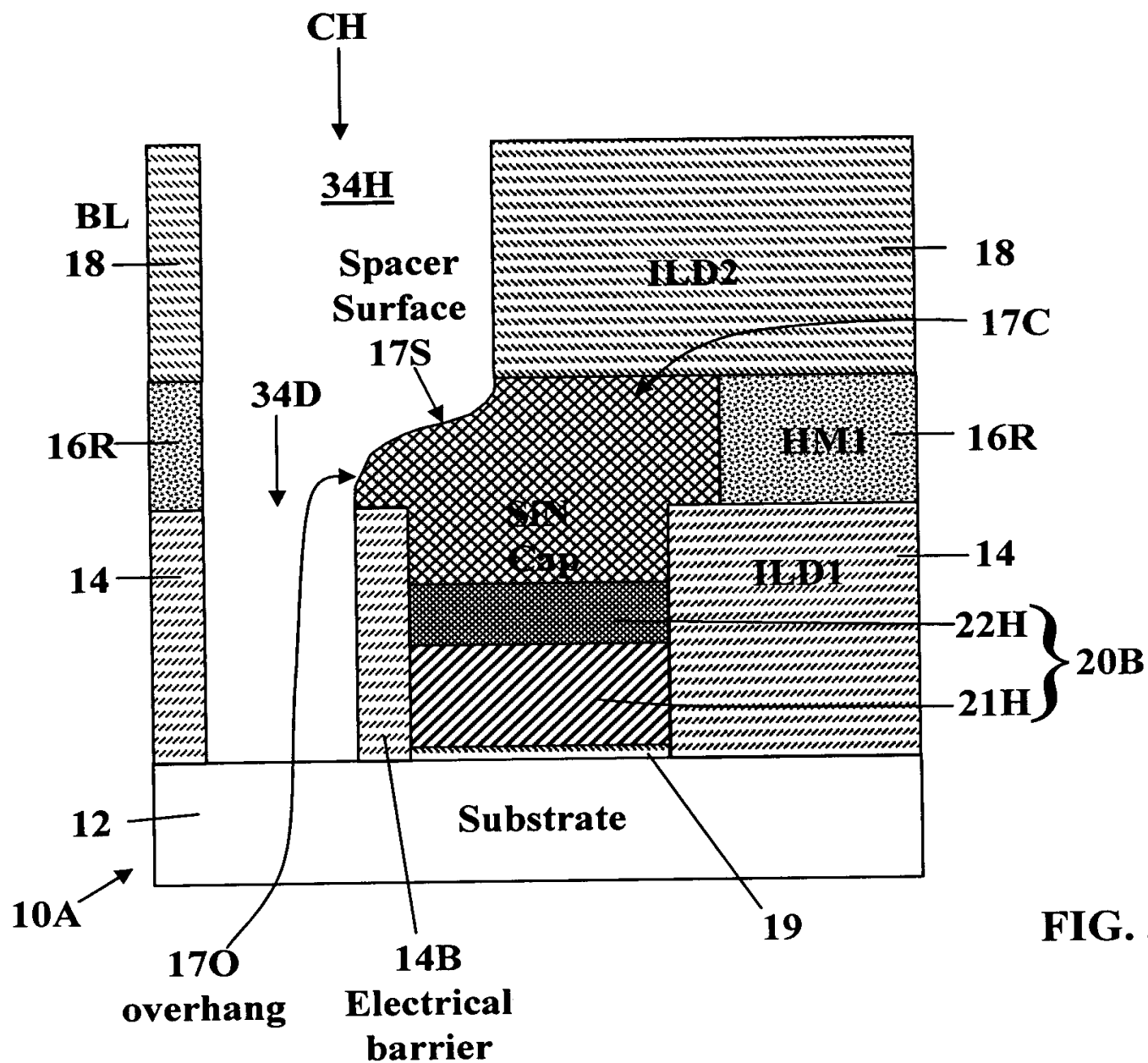
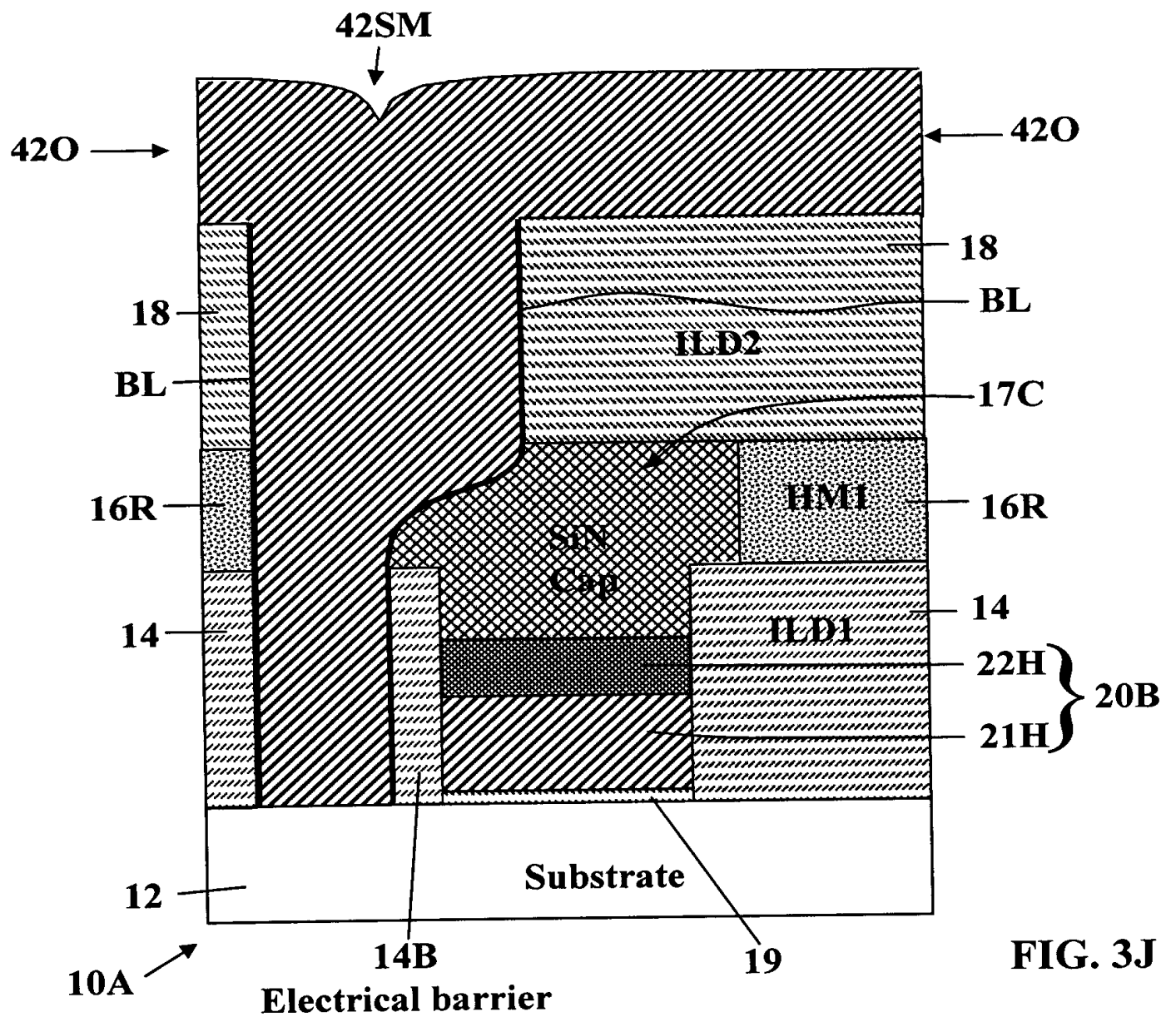
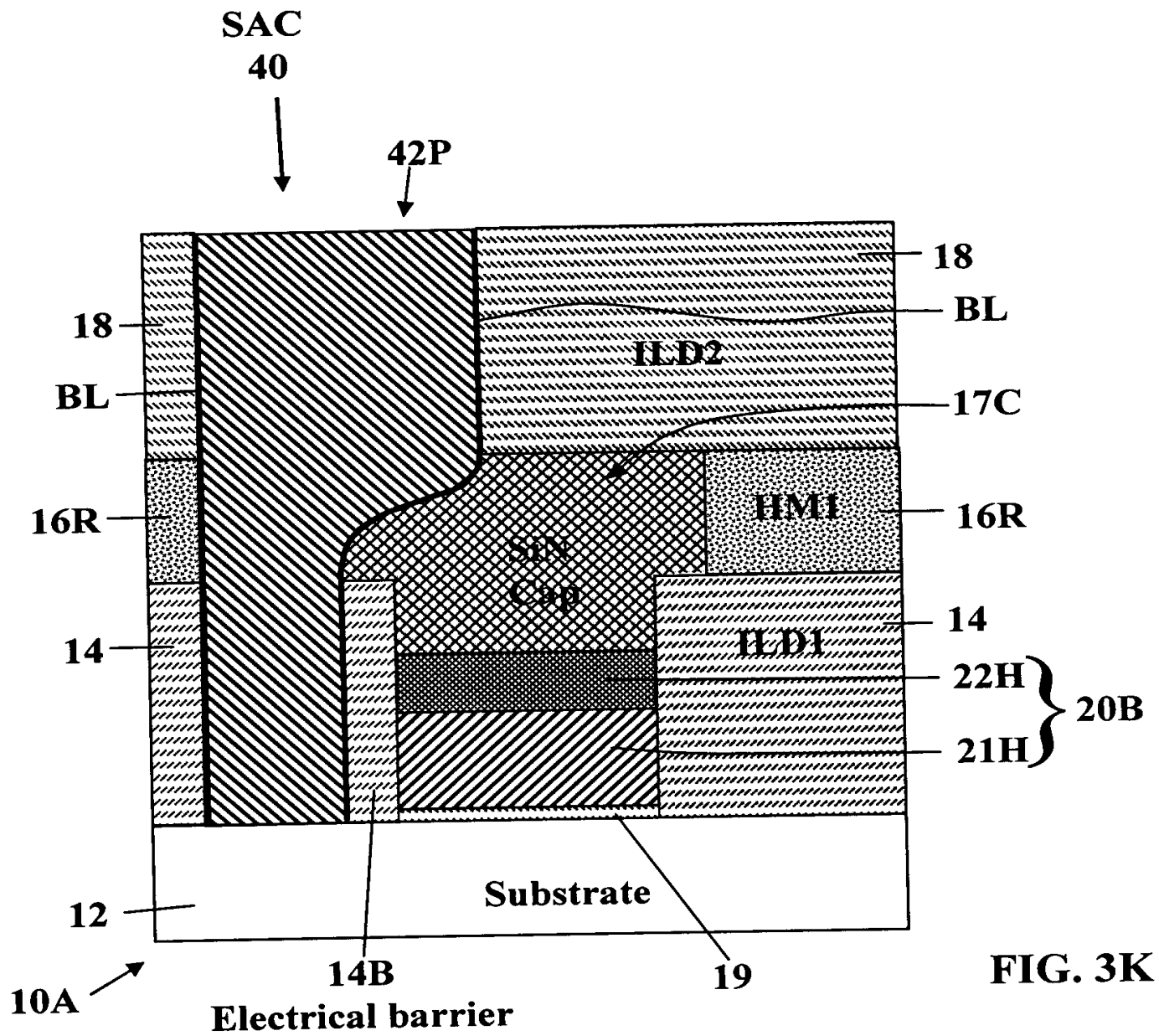


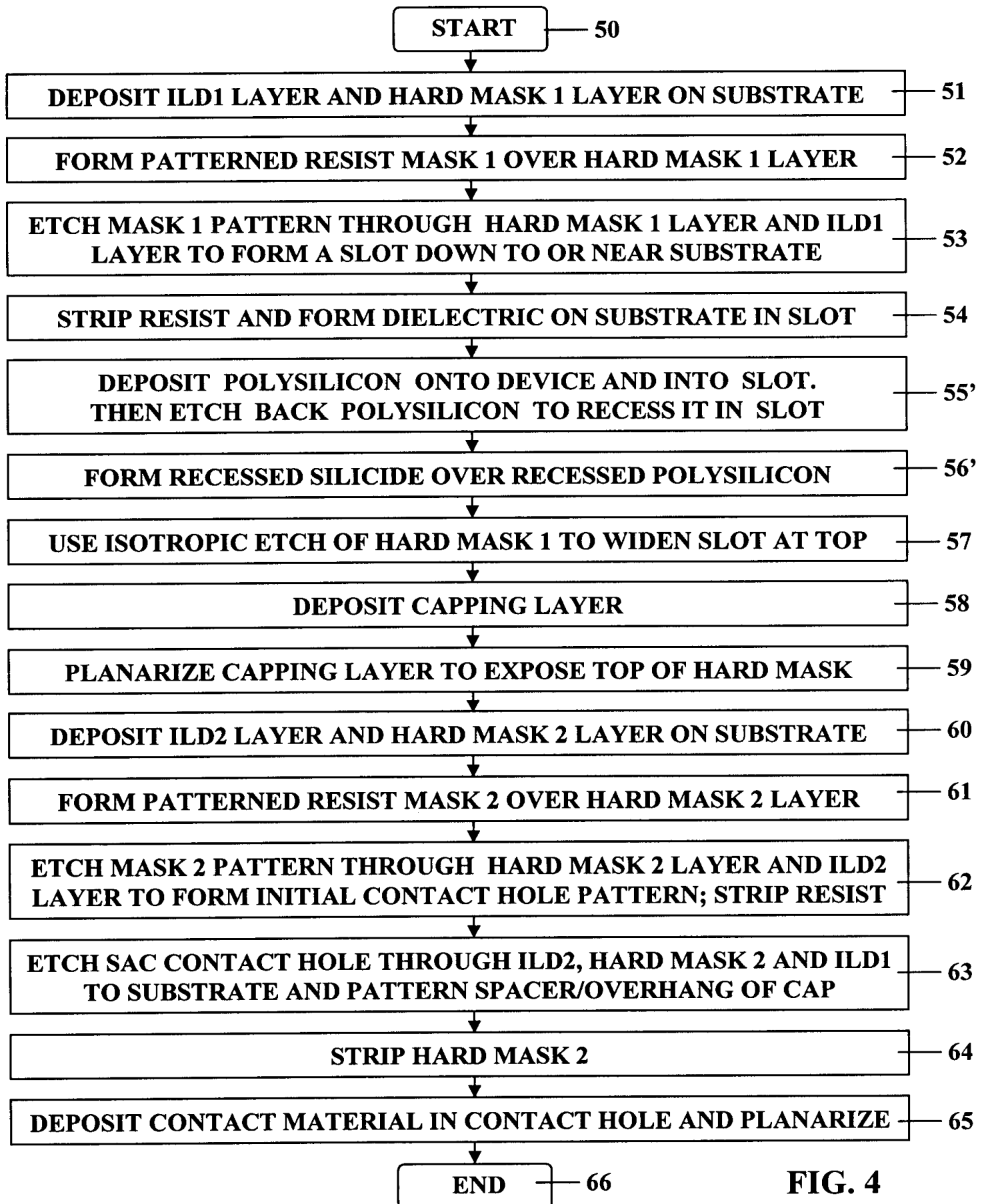
FIG. 3H

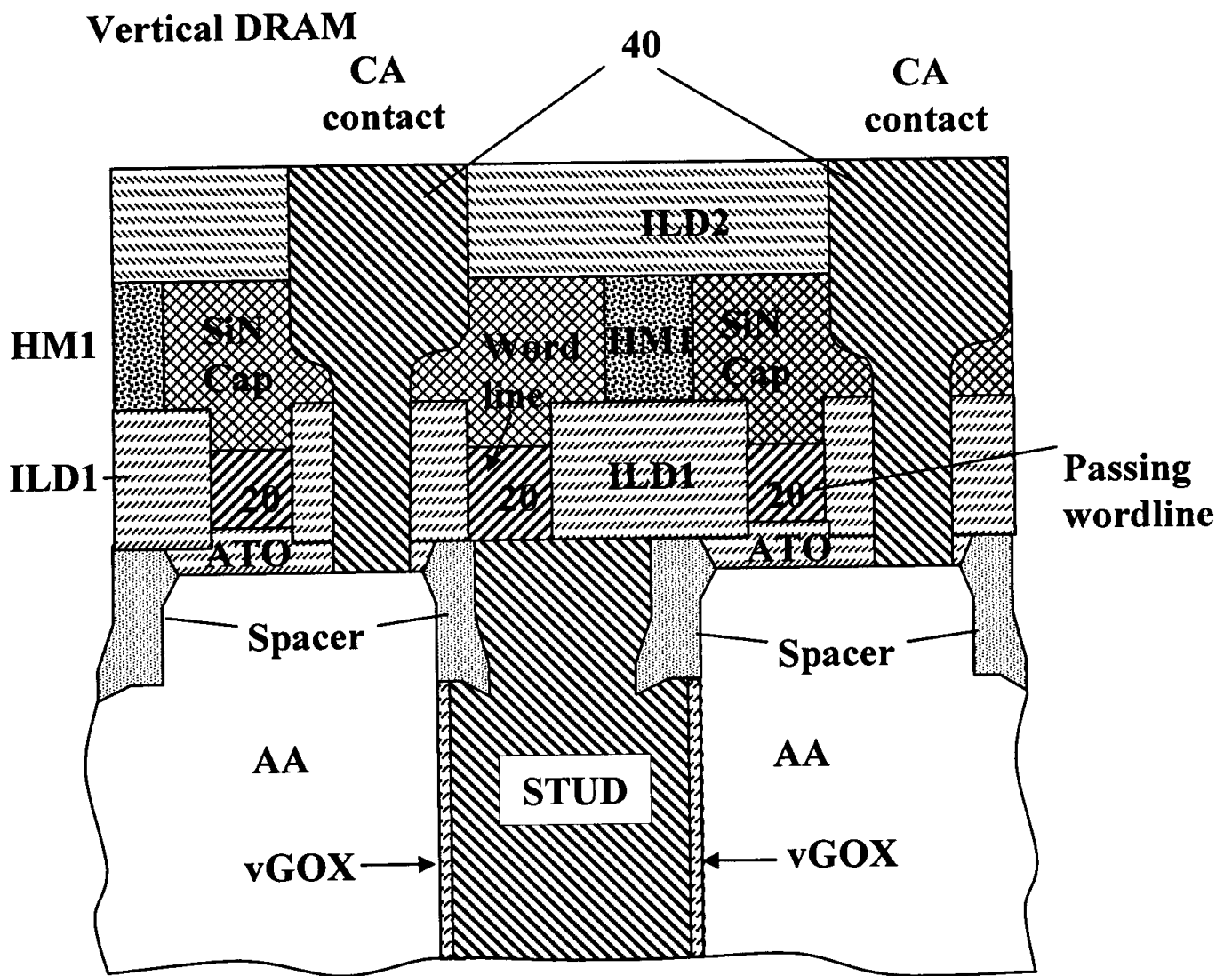






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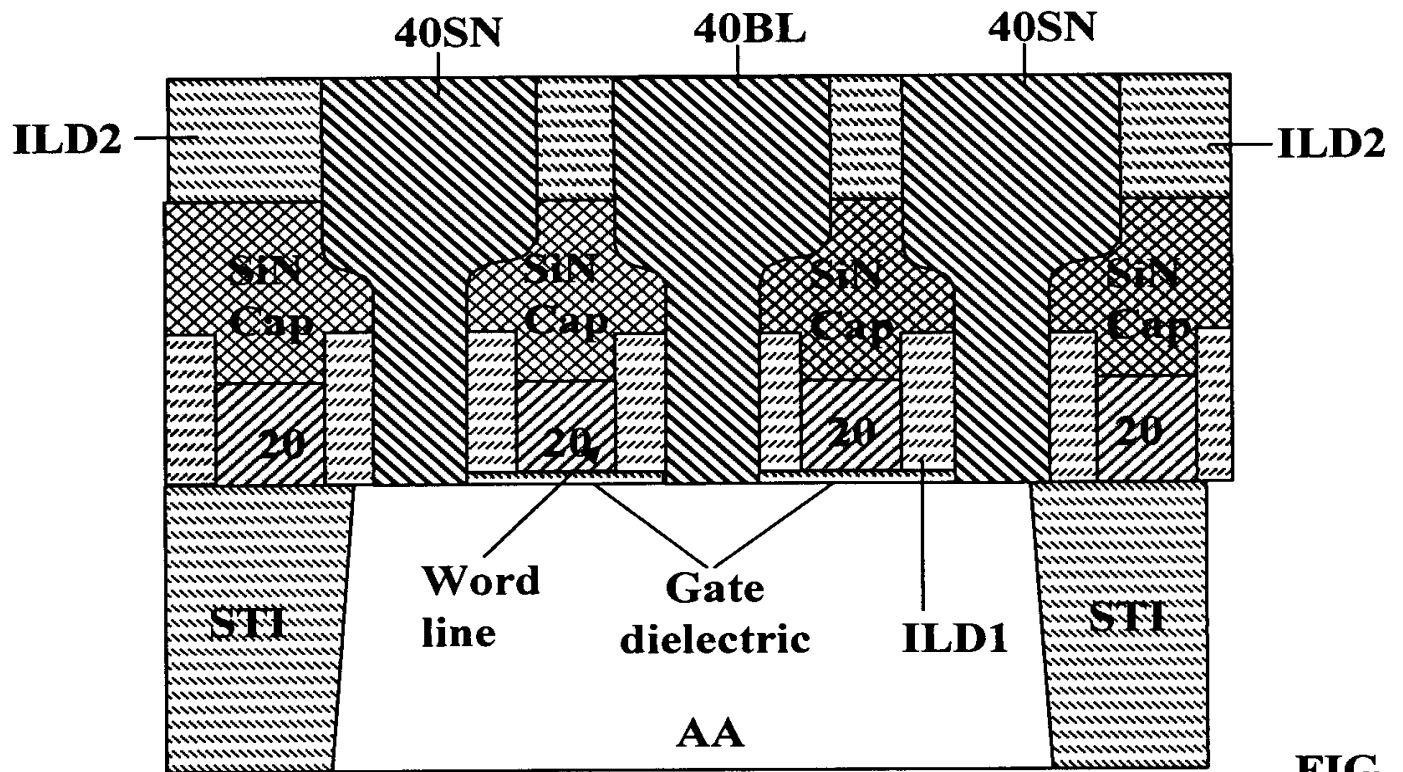
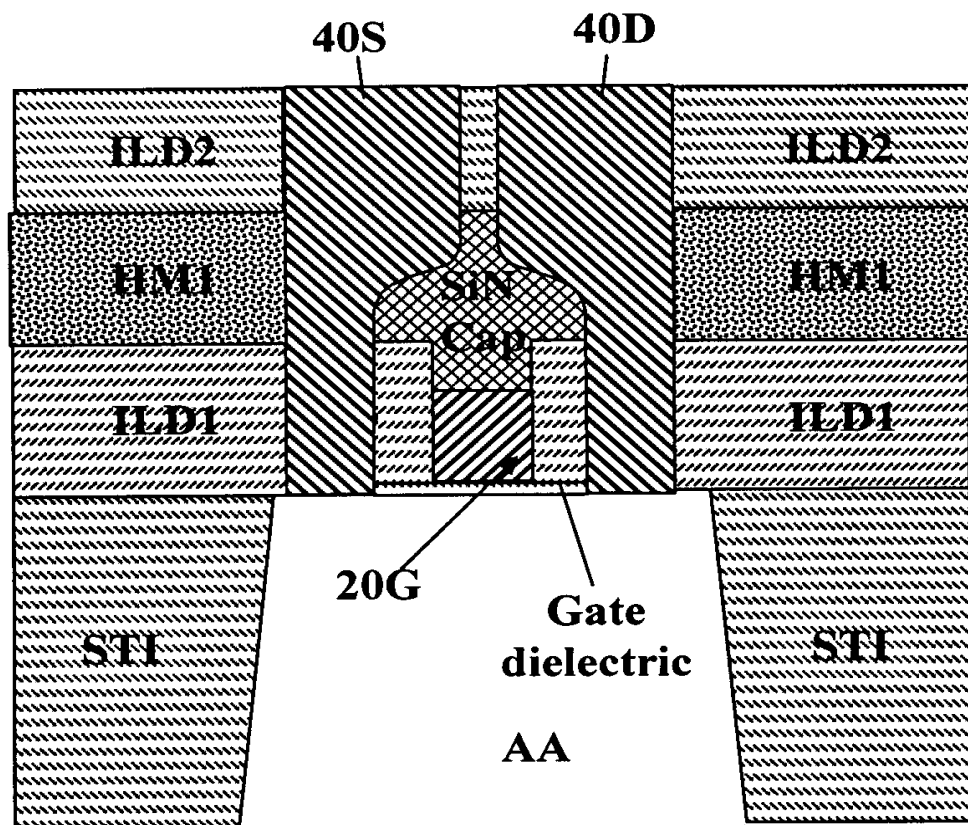
**FIG. 4**



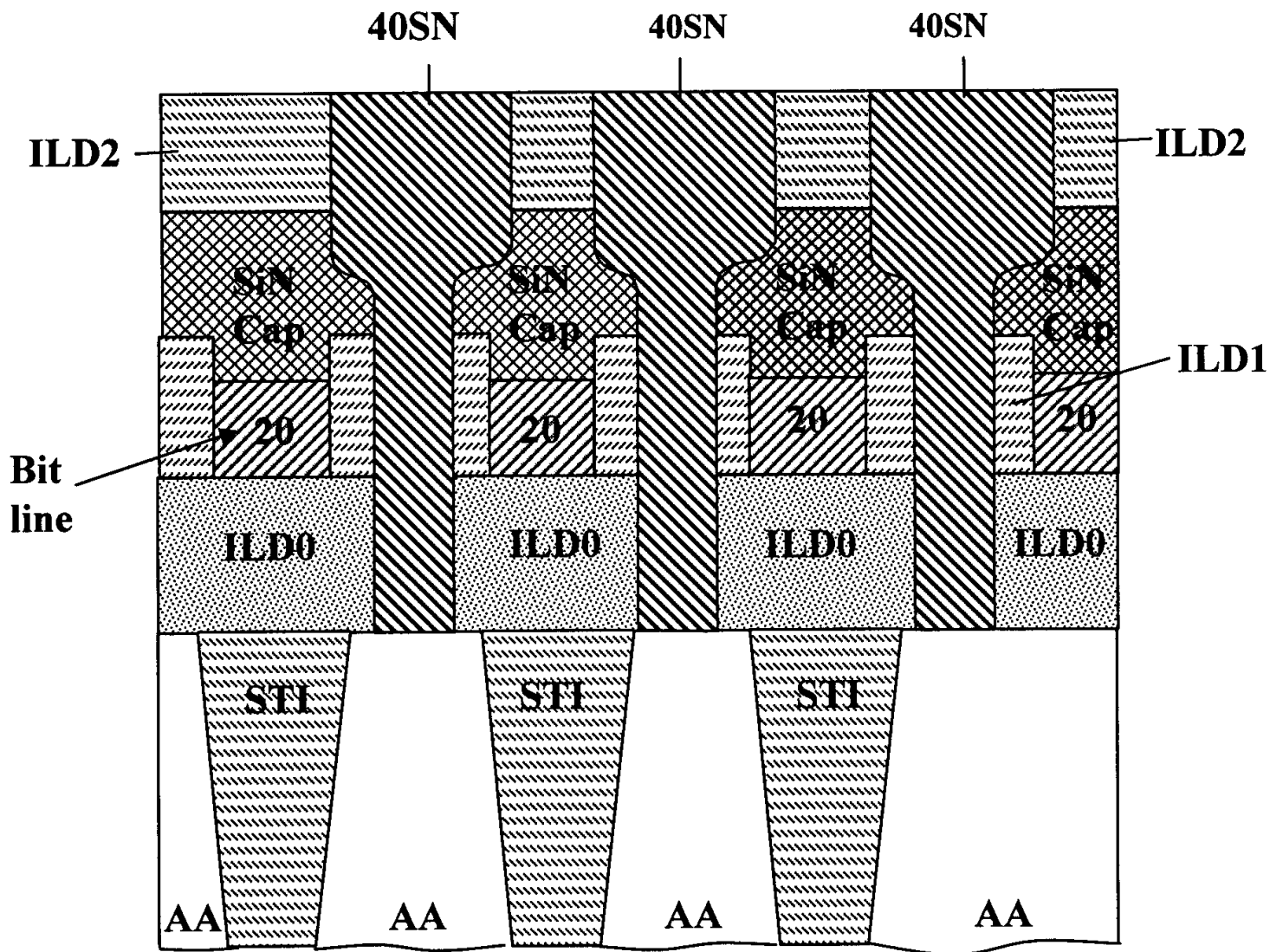
**FIG. 5**

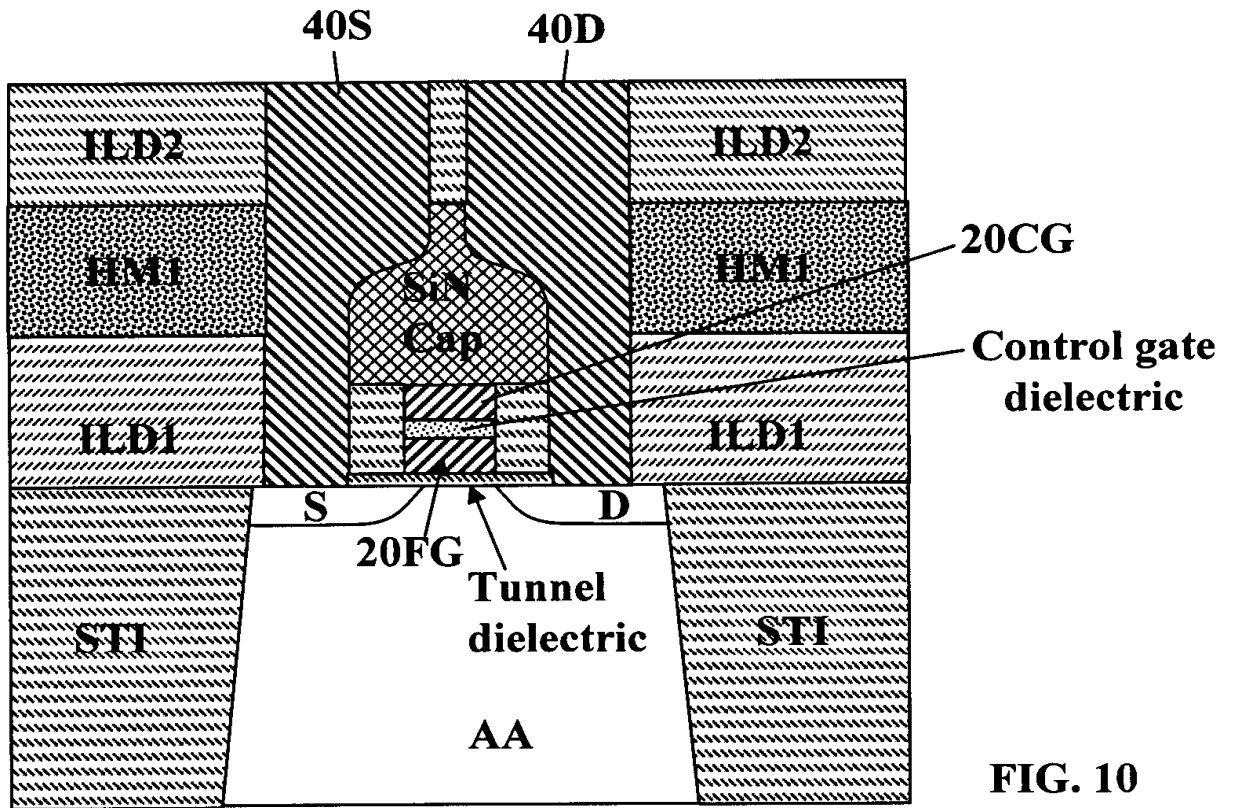
**FIG. 6**

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**Stack DRAM****FIG. 7****Metal Gate or SRAM****FIG. 8**

### Capacitor contact over bit line for stack DRAM

**FIG. 9**



### High Density Interconnect Line for BEOL

